The INRIA ZEP project: NVRAM and Harvesting for Zero Power Computations

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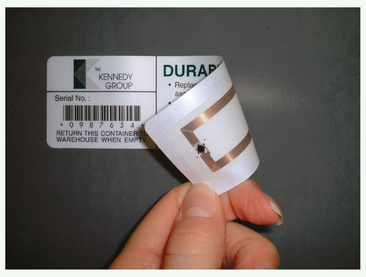
ZEP project: Context and Objectives



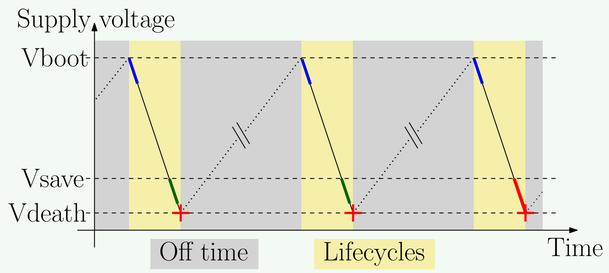


Figure: Examples of batteryless RFID tag and typical On/Off cycles of platforms supplied by energy harvesting, with checkpointing and restoration

Context

- The **Internet of Things** scenario predicts billions of communicating objects in a near future.
- **Maintenance cost** and **pollution issues** are major bottleneck for IoT.
- Emerging **non-volatile memory** (NVRAM) technologies and **harvesting** techniques predict new kinds of **batteryless embedded sensors**.
- **Checkpointing** [1] of platform state will be a central technique is these systems.

Challenges

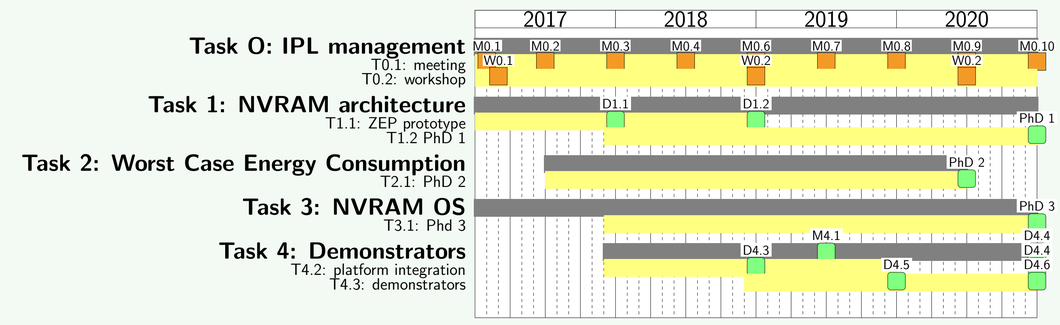
- Provide a new **computation model** adapted to NVRAM based micro-systems.
- Master **harvesting techniques** and energy control in ultra-low power domain.
- Provide real **computer science** contributions (langage, compiler, operating systems, etc...)
- Deliver innovative prototypes and a useful system-level simulators.

Partners and Methodology

Inria and CEA

- **Inria**, the French National Institute for computer science and applied mathematics, promotes scientific excellence for technology transfer and society. Inria is structured in research teams called project-teams.
- **CEA**, the French Alternative Energies and Atomic Energy Commission is a key player in technological research for industry. CEA research institutes (List and Leti) are structured in research teams called labs.
- Other institutes such as **Insa-Lyon** or **University of Rennes** are involved in Inria project-teams.
- The ZEP project is an **Inria Project Lab** (IPL), funded by Inria with more than 15 person-years hired over 4 years, including 3 PhDs. The Insa-Spie IoT Chair is also participating to the research effort of Citi Lab on IoT.

Planning



Teams and Skills

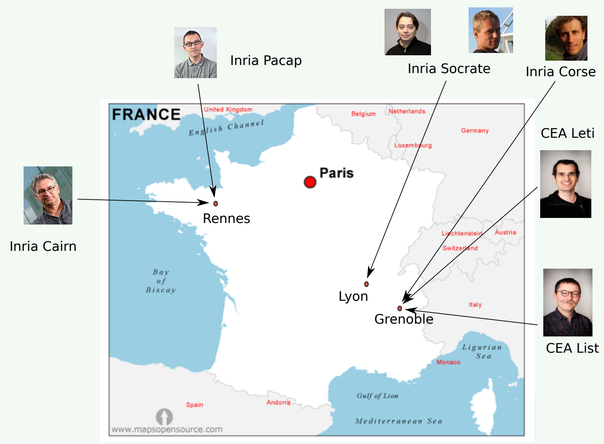


Figure: ZEP Teams involved with their correspondants scientists.

- **Inria Socrate** (Leader, `https://team.inria.fr/socrate/`): embedded system design, communication systems, operating systems and memory management [1].
- **Inria Cairn** (`https://team.inria.fr/cairn/`): energy-efficient system-on-chip and reconfigurable architecture, energy harvesting [2], compilers and design tools.
- **Inria Pacap** (`https://team.inria.fr/pacap/`): compiler optimization, compilation-time energy evaluation.
- **Inria Corse** (`https://team.inria.fr/corse/`): link between compilation and runtime.
- **CEA Leti** (Lisan, `http://www.leti-cea.fr/`): ultra-low power IOT platform [3].
- **CEA List** (Lialp, `http://www-list.cea.fr/`): just-in-time compilation.

Expected Results

After 4 years, the project should have achieved the following:

- A NVRAM based platform demonstrator powered by harvesting.
- An innovating NVRAM based processor architecture designed for VLSI integration.
- A solid system-level simulator for a generic NVRAM platform.
- A compiler leveraging WCEC (Worst Cases Energy Consumption) analysis.
- A primitive operating system including NVRAM management techniques and power management policies.
- Publications of course...
- Lobbying, communication, new research directions etc.

References

[1] Gautier Berthou, Tristan Delizy, Kevin Marquet, Tanguy Risset, and Guillaume Salagnac. "Peripheral state persistence for transiently-powered systems". In: *IoENT 2017 - 1st Workshop on Internet of Energy Neutral Things*. Geneva, Switzerland, June 2017.

[2] Olivier Berder and Olivier Sentieys. "PowWow: Power Optimized Hardware/Software Framework for Wireless Motes". In: *Workshop on Ultra-Low Power Sensor Networks (WUPS), co-located with Int. Conf. on Architecture of Computing Systems (ARCS 2010)*. Hannover, Germany, Feb. 2010, pp. 229–233.

[3] Edith Beign et al. "L-IOT: a Flexible Energy Efficient Platform Targeting Wide Range IoT Applications". In: *ACM/EDAC/IEEE Design Automation Conference (DAC)*. Austin, TX, 2017.

Work Packages

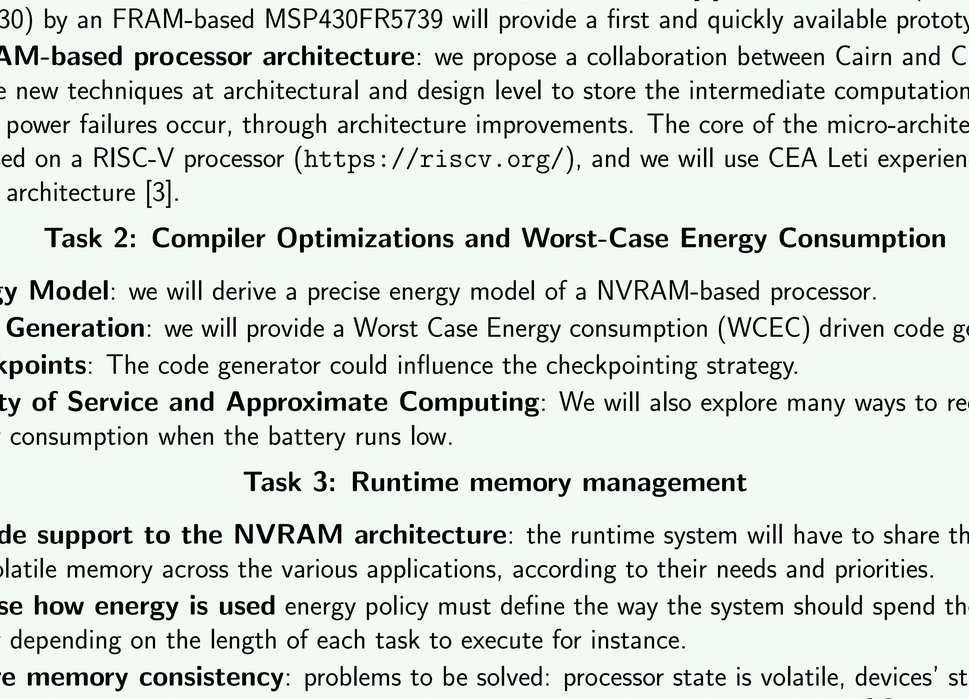


Figure: Overview of the ZEP resulting prototype

Task1: NVRAM-based Architecture

- **NVRAM technology study**: This expertise is mandatory to always consider that the proposed non-volatile processor is feasible in terms of technology
- **NVRAM-based sensor node platform**: Replacing the PowWow [2] micro-controller (currently an MSP430) by an FRAM-based MSP430FR5739 will provide a first and quickly available prototype.
- **NVRAM-based processor architecture**: we propose a collaboration between Cairn and CEA Leti to explore new techniques at architectural and design level to store the intermediate computation states before power failures occur, through architecture improvements. The core of the micro-architecture will be based on a RISC-V processor (`https://riscv.org/`), and we will use CEA Leti experience on the L-IOT architecture [3].

Task 2: Compiler Optimizations and Worst-Case Energy Consumption

- **Energy Model**: we will derive a precise energy model of a NVRAM-based processor.
- **Code Generation**: we will provide a Worst Case Energy consumption (WCEC) driven code generation .
- **Checkpoints**: The code generator could influence the checkpointing strategy.
- **Quality of Service and Approximate Computing**: We will also explore many ways to reduce energy consumption when the battery runs low.

Task 3: Runtime memory management

- **Provide support to the NVRAM architecture**: the runtime system will have to share the non-volatile memory across the various applications, according to their needs and priorities.
- **Choose how energy is used** energy policy must define the way the system should spend the available energy depending on the length of each task to execute for instance.
- **Ensure memory consistency**: problems to be solved: processor state is volatile, devices' states are volatile and a priority between applications when saving data of must be established [1].

Task 4: Experimental platforms and use cases

- **Use cases**: Use cases will include a sensing application, a cryptography application, and a video decoding application.
- **Experimental platform**: the **ZEP prototype** will consist in the integration of recent FRAM MSP430 from Texas Instrument (MSP430FR5739 for instance) integrated in a new version of the PowWow sensor [2] node in which an the Actel Igloo FPGA also includes NVRAM.
- **Simulation platform**: for more advanced design issues, we will use simulation tools provided by CEA (for L-IOT) and other vendors for NVRAM to provide a precise system-level simulator