



# High-level synthesis and arithmetic optimizations

Yohann Uguen, Florent de Dinechin, Steven Derrien

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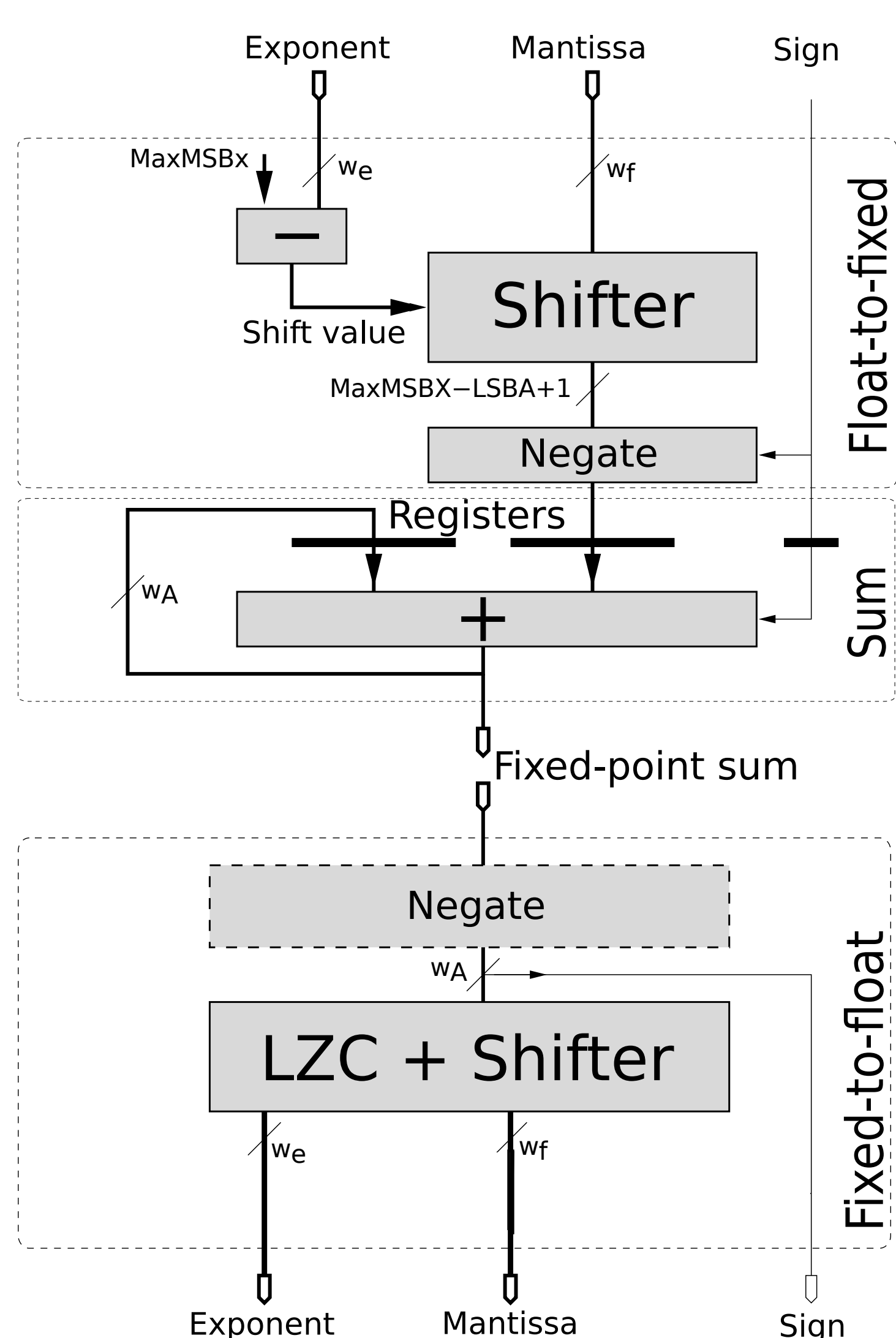
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## CONTEXT

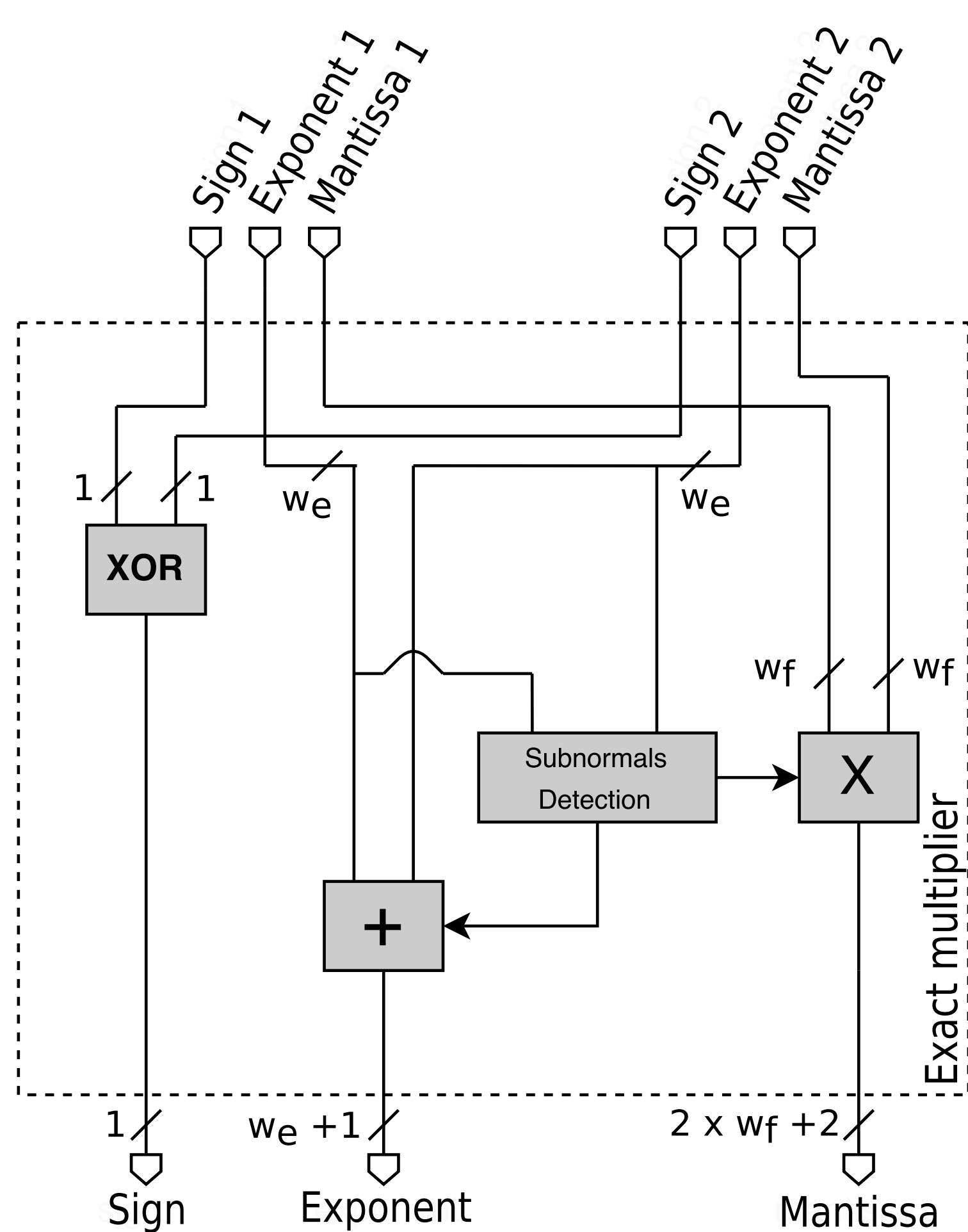
- Computing with real numbers
- Design a hardware accelerator
- Targeting FPGAs
- Trade off between
  1. performance
  2. accuracy
  3. resource usage
  4. ease of use

## ACCUMULATOR

Based on Kulisch and Snyder accumulator [3]



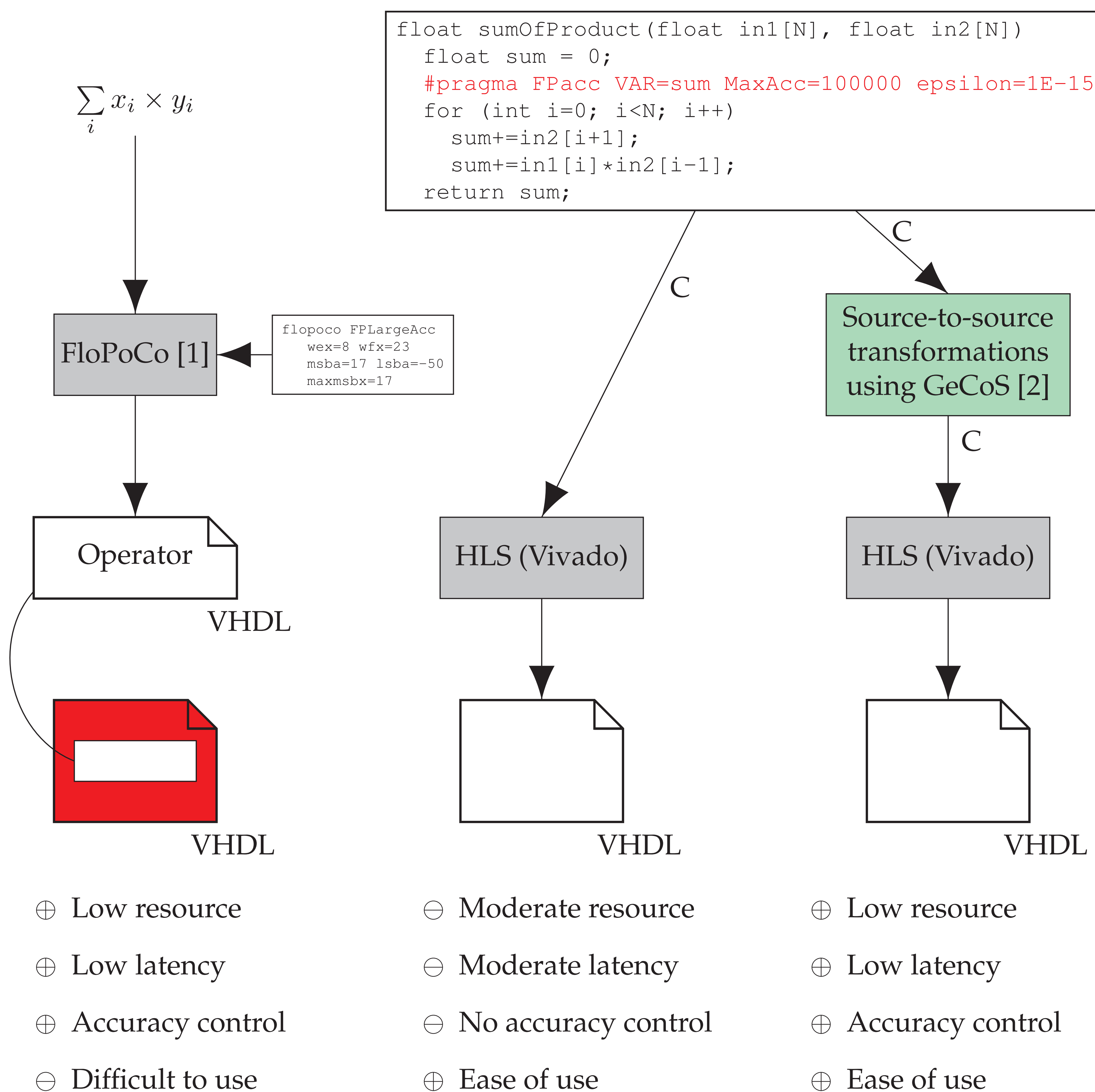
## EXACT MULTIPLIER



## REFERENCES

- [1] de Dinechin, Florent et al.: *An FPGA-specific Approach to Floating-Point Accumulation and Sum-of-Products*, FPT 2008
- [2] Floc'h, Antoine et al.: *GeCoS: A framework for prototyping custom hardware design flows*, SCAM 2013
- [3] Kulisch, Ulrich and Snyder, Van: *The Exact Dot Product As Basic Tool for Long Interval Arithmetic*, Computing 2011

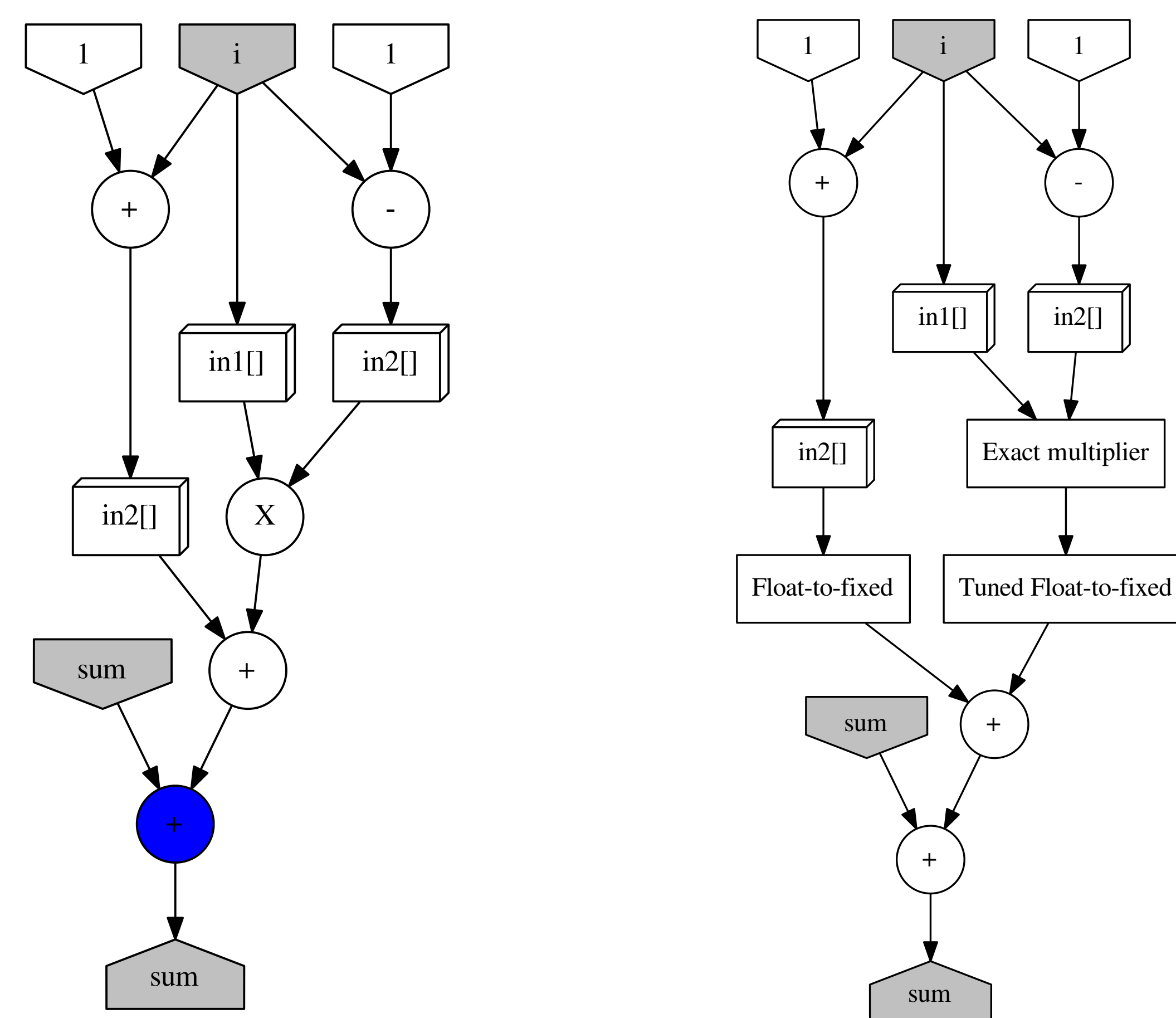
## MERGING APPLICATION-SPECIFIC ARITHMETIC AND HLS



## SOURCE-TO-SOURCE TRANSFORMATIONS USING GECoS

```

switch Node do
  case +
    | Launch recursively
      on incoming nodes
  end case
  case ×
    | Replace with exact
      multiplier
      combined with
      tuned
      Float-to-fixed
      operator
  end case
  case Accumulation
    variable
    | Ignore
  end case
  otherwise
    | Insert
      Float-to-fixed node
  end
endsw
    
```



## RESULTS

Input values in [0, 1]  
 100K accumulations

	FloPoCo's Operator	Naive Code	Transformed Code
Accumulator width	67	24	67
LUTs	693	313	868
DSPs	2	5	2
Latency	100K	1000K	100K
Accuracy	24 bits	17 bits	24 bits