

VLSI-SoC: Design and Engineering of Electronics Systems Based on New Computing Paradigms

Nicola Bombieri, Graziano Pravadelli, Masahiro Fujita, Todd Austin, Ricardo Reis

► **To cite this version:**

Nicola Bombieri, Graziano Pravadelli, Masahiro Fujita, Todd Austin, Ricardo Reis. VLSI-SoC: Design and Engineering of Electronics Systems Based on New Computing Paradigms: 26th IFIP WG 10.5/IEEE International Conference on Very Large Scale Integration, VLSI-SoC 2018, Verona, Italy, October 8–10, 2018, Revised and Extended Selected Papers. Springer International Publishing, AICT-561, 2019, IFIP Advances in Information and Communication Technology, 978-3-030-23424-9. 10.1007/978-3-030-23425-6 . hal-02315625

HAL Id: hal-02315625

<https://hal.inria.fr/hal-02315625>

Submitted on 14 Oct 2019

HAL is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.



Editor-in-Chief

Kai Rannenberg, Goethe University Frankfurt, Germany

Editorial Board Members

TC 1 – Foundations of Computer Science

Jacques Sakarovitch, Télécom ParisTech, France

TC 2 – Software: Theory and Practice

Michael Goedicke, University of Duisburg-Essen, Germany

TC 3 – Education

Arthur Tatnall, Victoria University, Melbourne, Australia

TC 5 – Information Technology Applications

Erich J. Neuhold, University of Vienna, Austria

TC 6 – Communication Systems

Aiko Pras, University of Twente, Enschede, The Netherlands

TC 7 – System Modeling and Optimization

Fredi Tröltzsch, TU Berlin, Germany

TC 8 – Information Systems

Jan Pries-Heje, Roskilde University, Denmark

TC 9 – ICT and Society

David Kreps, University of Salford, Greater Manchester, UK

TC 10 – Computer Systems Technology

Ricardo Reis, Federal University of Rio Grande do Sul, Porto Alegre, Brazil

TC 11 – Security and Privacy Protection in Information Processing Systems

Steven Furnell, Plymouth University, UK

TC 12 – Artificial Intelligence

Ulrich Furbach, University of Koblenz-Landau, Germany

TC 13 – Human-Computer Interaction

Marco Winckler, University of Nice Sophia Antipolis, France

TC 14 – Entertainment Computing

Rainer Malaka, University of Bremen, Germany

IFIP – The International Federation for Information Processing

IFIP was founded in 1960 under the auspices of UNESCO, following the first World Computer Congress held in Paris the previous year. A federation for societies working in information processing, IFIP's aim is two-fold: to support information processing in the countries of its members and to encourage technology transfer to developing nations. As its mission statement clearly states:

IFIP is the global non-profit federation of societies of ICT professionals that aims at achieving a worldwide professional and socially responsible development and application of information and communication technologies.

IFIP is a non-profit-making organization, run almost solely by 2500 volunteers. It operates through a number of technical committees and working groups, which organize events and publications. IFIP's events range from large international open conferences to working conferences and local seminars.

The flagship event is the IFIP World Computer Congress, at which both invited and contributed papers are presented. Contributed papers are rigorously refereed and the rejection rate is high.

As with the Congress, participation in the open conferences is open to all and papers may be invited or submitted. Again, submitted papers are stringently refereed.

The working conferences are structured differently. They are usually run by a working group and attendance is generally smaller and occasionally by invitation only. Their purpose is to create an atmosphere conducive to innovation and development. Refereeing is also rigorous and papers are subjected to extensive group discussion.

Publications arising from IFIP events vary. The papers presented at the IFIP World Computer Congress and at open conferences are published as conference proceedings, while the results of the working conferences are often published as collections of selected and edited papers.

IFIP distinguishes three types of institutional membership: Country Representative Members, Members at Large, and Associate Members. The type of organization that can apply for membership is a wide variety and includes national or international societies of individual computer scientists/ICT professionals, associations or federations of such societies, government institutions/government related organizations, national or international research institutes or consortia, universities, academies of sciences, companies, national or international associations or federations of companies.

More information about this series at <http://www.springer.com/series/6102>

Nicola Bombieri · Graziano Pravadelli ·
Masahiro Fujita · Todd Austin ·
Ricardo Reis (Eds.)

VLSI-SoC: Design and Engineering of Electronics Systems Based on New Computing Paradigms

26th IFIP WG 10.5/IEEE International Conference
on Very Large Scale Integration, VLSI-SoC 2018
Verona, Italy, October 8–10, 2018
Revised and Extended Selected Papers

Editors

Nicola Bombieri
University of Verona
Verona, Italy

Masahiro Fujita
University of Tokyo
Tokyo, Japan

Ricardo Reis
Universidade Federal do Rio Grande
do Sul
Porto Alegre, Brazil

Graziano Pravadelli
University of Verona
Verona, Italy

Todd Austin
University of Michigan
Ann Arbor, MI, USA

ISSN 1868-4238 ISSN 1868-422X (electronic)
IFIP Advances in Information and Communication Technology
ISBN 978-3-030-23424-9 ISBN 978-3-030-23425-6 (eBook)
<https://doi.org/10.1007/978-3-030-23425-6>

© IFIP International Federation for Information Processing 2019

This work is subject to copyright. All rights are reserved by the Publisher, whether the whole or part of the material is concerned, specifically the rights of translation, reprinting, reuse of illustrations, recitation, broadcasting, reproduction on microfilms or in any other physical way, and transmission or information storage and retrieval, electronic adaptation, computer software, or by similar or dissimilar methodology now known or hereafter developed.

The use of general descriptive names, registered names, trademarks, service marks, etc. in this publication does not imply, even in the absence of a specific statement, that such names are exempt from the relevant protective laws and regulations and therefore free for general use.

The publisher, the authors and the editors are safe to assume that the advice and information in this book are believed to be true and accurate at the date of publication. Neither the publisher nor the authors or the editors give a warranty, expressed or implied, with respect to the material contained herein or for any errors or omissions that may have been made. The publisher remains neutral with regard to jurisdictional claims in published maps and institutional affiliations.

This Springer imprint is published by the registered company Springer Nature Switzerland AG
The registered company address is: Gewerbestrasse 11, 6330 Cham, Switzerland

Preface

This book contains extended and revised versions of the highest-quality papers presented during the 26th edition of the IFIP/IEEE WG10.5 International Conference on Very Large Scale Integration (VLSI-SoC), a global System-on-Chip Design and CAD conference. The 26th edition of the conference was held during October 8–10, 2018, at the Hotel Leon d’Oro, Verona, Italy. Previous conferences have taken place in Edinburgh, Scotland (1981); Trondheim, Norway (1983); Tokyo, Japan (1985); Vancouver, Canada (1987); Munich, Germany (1989); Edinburgh, Scotland (1991); Grenoble, France (1993); Chiba, Japan (1995); Gramado, Brazil (1997); Lisbon, Portugal (1999); Montpellier, France (2001); Darmstadt, Germany (2003); Perth, Australia (2005); Nice, France (2006); Atlanta, GA, USA (2007); Rhodes Island, Greece (2008); Florianopolis, Brazil (2009); Madrid, Spain (2010); Kowloon, Hong Kong, SAR China (2011), Santa Cruz, CA, USA (2012), Istanbul, Turkey (2013), Playa del Carmen, Mexico (2014), Daejeon, South Korea (2015), Tallin, Estonia (2016), and Abu Dhabi, United Arab Emirates (2017).

The purpose of this conference, sponsored by IFIP TC 10 Working Group 10.5, the IEEE Council on Electronic Design Automation (CEDA), and the IEEE Circuits and Systems Society, with the In-Cooperation of ACM SIGDA, is to provide a forum for the presentation and discussion of the latest academic and industrial results and developments as well as the future trends in the field of system-on-chip (SoC) design, considering the challenges of nano-scale, state-of-the-art and emerging manufacturing technologies. In particular, VLSI-SoC 2018 was held under the theme “Design and Engineering of Electronics Systems Based on New Computing Paradigms” by addressing cutting-edge research fields like heterogeneous, neuromorphic, and brain-inspired, biologically inspired, approximate computing systems. The chapters of this new book in the VLSI-SoC series continue its tradition of providing an internationally acknowledged platform for scientific contributions and industrial progress in this field.

For VLSI-SoC 2018, 27 papers out of 106 submissions were selected for presentation, and out of these 27 full papers presented at the conference, 13 papers were chosen by a special selection committee to have an extended and revised version included in this book. The selection process of these papers considered the evaluation scores during the review process as well as the review forms provided by members of the Technical Program Committee and the Session Chairs as a result of the presentations.

The chapters of this book have authors from Germany, India, Italy, Japan, Mexico, Singapore, The Netherlands, UAE, and USA. The Technical Program Committee for the regular tracks comprised 98 members from 25 countries.

VLSI-SoC 2018 was the culmination of the work of many dedicated volunteers: paper authors, reviewers, session chairs, invited speakers, and various committee chairs. We thank them all for their contributions.

This book is intended for the VLSI community at large, and in particular the many colleagues who did not have the chance to attend the conference. We hope you will enjoy reading this book and that you will find it useful in your professional life and for the development of the VLSI community as a whole.

June 2019

Nicola Bombieri
Graziano Pravadelli
Masahiro Fujita
Todd Austin
Ricardo Reis

Organization

The IFIP/IEEE International Conference on Very Large Scale Integration System-on-Chip (VLSI-SoC) 2018 took place during October 8–10, 2018, at the Hotel Leon d’Oro, Verona, Italy. VLSI-SoC 2018 was the 26th in a series of international conferences, sponsored by IFIP TC 10 Working Group 10.5 (VLSI), IEEE CEDA and ACM SIGDA.

General Chairs

Graziano Pravadelli	University of Verona, Italy
Todd Austin	University of Michigan, USA

Technical Program Chairs

Nicola Bombieri	University of Verona, Italy
Masahiro Fujita	University of Tokyo, Japan

Special Sessions Chairs

Sirivas Katkooi	University of South Florida, USA
Katell Morin-Allory	TIMA Laboratory, France

PhD Forum Chairs

Kiyoung Choi	Seoul National University, South Korea
Sara Vinco	Politecnico di Torino, Italy

Local Chair

Franco Fummi	University of Verona, Italy
--------------	-----------------------------

Industry Chair

Yervant Zorian	Synopsys, USA (TBC)
----------------	---------------------

Publicity Chairs

Ricardo Reis	UFRGS, Brazil
Matteo Sonza Reorda	Politecnico di Torino, Italy

VLSI-SoC Steering Committee

Manfred Glesner	TU Darmstadt, Germany
Matthew Guthaus	UC Santa Cruz, USA
Luis Miguel Silveira	INESC ID, Portugal
Fatih Ugurdag	Ozyegin University, Turkey
Salvador Mir	TIMA, France
Ricardo Reis	UFRGS, Brazil
Chi-Ying Tsui	HKUST, Hong Kong, SAR China
Ian O'Connor	INL, France
Masahiro Fujita	The University of Tokyo, Japan

Publication Chairs

Davide Bertozzi	University of Ferrara, Italy
Mahdi Tala	University of Ferrara, Italy

Registration Chair

Michele Lora	Singapore University of Technology and Design, Singapore
--------------	---

Web Chair

Florenc Demrozi	University of Verona, Italy
-----------------	-----------------------------

Technical Program Committee

Analog, Mixed-Signal, and Sensor Architectures

Track Chairs

Piero Malcovati	University of Pavia, Italy
Tetsuya Iizuka	University of Tokyo, Japan

Digital Architectures: NoC, Multi- and Many-Core, Hybrid, and Reconfigurable

Track Chairs

Ian O'Connor	Lyon Institute of Nanotechnology, France
Michael Huebner	Ruhr-Universität Bochum, Germany

CAD, Synthesis, and Analysis

Track Chairs

Srinivas Katkoori	University of South Florida, USA
Ibrahim Elfadel	Masdar Institute, UAE

Prototyping, Verification, Modeling, and Simulation

Track Chairs

Tiziana Margaria	Lero, Ireland
Katell Morin-Allory	Grenoble Institute of Technology, France

Circuits and Systems for Signal Processing and Communications

Track Chairs

Fatih Ugurdag	Ozyegin University, Turkey
Luc Claesen	Hasselt University, Belgium

IoT, Embedded and Cyberphysical Systems: Architecture, Design, and Software

Track Chairs

Zebo Peng	Linkoping University, Sweden
Donatella Sciuto	Politecnico di Milano, Italy

Low-Power and Thermal-Aware IC Design

Track Chairs

Dimitrios Soudris	National Technical University of Athens NTUA, Greece
Alberto Macii	Politecnico di Torino, Italy

Emerging Technologies and Computing Paradigms

Track Chairs

Andrea Calimera	Politecnico di Torino, Italy
Ricardo Reis	UFRGS, Brazil

Variability, Reliability, and Test

Track Chairs

Salvador Mir	University of Grenoble Alpes, France
Matteo Sonza Reorda	Politecnico di Torino, Italy

Jaan Raik	Tallin University, Estonia
Jones Yudi Mori	University of Brasilia, Brazil
Jinmyoung Kim	Samsung Advanced Institute of USA, Technology, South Korea
Johanna Sepulveda	Technical University of Munich, Germany
Jose Monteiro	INESC-ID, IST University of Lisbon, Portugal
Ke Huang	San Diego State University, USA
Kostas Siozios	Aristotle University of Thessaloniki, Greece
Lars Bauer	Karlsruhe Institute of Technology, Germany
Leandro Indrusiak	University of York, UK
Lionel Torres	LIRMM, France
Luciano Ost	University of Leicester, UK
Maksim Jenihhin	Tallinn University of Technology, Estonia
Maria Michael	University of Cyprus, Cyprus
Massimo Poncino	Politecnico di Torino, Italy
Matthias Sauer	University Freiburg, Germany
Mirko Loghi	Università di Udine, Italy
Nadine Azemard	LIRMM/CNRS, France
Nele Mentens	Katholieke Universiteit Leuven, Belgium
Nektarios Georgios Tsoutsos	New York University, USA
Ozgur Tasdizen	ARM, UK
Paolo Amato	Micron, Italy
Patri Sreehari	National Institute of Technology, Warangal, India
Peng Liu	Zhejiang University, China
Per Larsson-Edefors	Chalmers University, Sweden
Philippe Coussy	Université de Bretagne, France
Pierre-Emmanuel Gaillardon	University of Utah, USA
Po-Hung Chen	National Chiao Tung University, Taiwan
Raik Brinkmann	OneSpin Solutions, Germany
Rani S. Ghaida	Global Foundries, USA
Robert Wille	Johannes Kepler University Linz, Austria
Rouwaida Kanj	American University of Beirut, Lebanon
Said Hamdioui	Delft Technical University, The Netherlands
Salvatore Pennisi	University of Catania, Italy
Sezer Goren	Yeditepe University, Turkey
Shahar Kvatinsky	Technion - Israel Institute of Technology, Israel
Sicheng Li	HP, USA
Soheil Samii	General Motors, USA
Sri Parameswaran	University of New South Wales, Australia
Tetsuya Hirose	Kobe University, Japan
Theocharis Theocharides	University of Cyprus, Cyprus
Tolga Yalcin	NXP, UK
Valerio Tenace	Politecnico di Torino, Italy

Victor Champac	National Institute of Astrophysics, Optics and Electronics, Mexico
Victor Kravets	IBM, USA
Virendra Singh	Indian Institute of Technology Bombay, India
Vladimir Zolotov	IBM, USA
Wenjing Rao	University of Illinois at Chicago, USA
Yier Jin	University of Florida, USA

Contents

A 65 nm CMOS Synthesizable Digital Low-Dropout Regulator Based on Voltage-to-Time Conversion with 99.6% Current Efficiency at 10-mA Load	1
<i>Naoki Ojima, Toru Nakura, Tetsuya Iizuka, and Kunihiro Asada</i>	
An Instruction Set Architecture for Secure, Low-Power, Dynamic IoT Communication.	14
<i>Shahzad Muzaffar and Ibrahim (Abe) M. Elfadel</i>	
The Connection Layout in a Lattice of Four-Terminal Switches	32
<i>Anna Bernasconi, Antonio Boffa, Fabrizio Luccio, and Linda Pagli</i>	
Building High-Performance, Easy-to-Use Polymorphic Parallel Memories with HLS.	53
<i>L. Stornaiuolo, M. Rabozzi, M. D. Santambrogio, D. Sciuto, C. B. Ciobanu, G. Stramondo, and A. L. Varbanescu</i>	
Rectification of Arithmetic Circuits with Craig Interpolants in Finite Fields	79
<i>Utkarsh Gupta, Irina Iliaeva, Vikas Rao, Arpitha Srinath, Priyank Kalla, and Florian Enescu</i>	
Energy-Accuracy Scalable Deep Convolutional Neural Networks: A Pareto Analysis	107
<i>Valentino Peluso and Andrea Calimera</i>	
ReRAM Based In-Memory Computation of Single Bit Error Correcting BCH Code.	128
<i>Swagata Mandal, Yaswanth Tavva, Debjyoti Bhattacharjee, and Anupam Chattopadhyay</i>	
Optimizing Performance and Energy Overheads Due to Fanout in In-Memory Computing Systems	147
<i>Md Adnan Zaman, Rajeev Joshi, and Srinivas Katkoori</i>	
Mapping Spiking Neural Networks on Multi-core Neuromorphic Platforms: Problem Formulation and Performance Analysis	167
<i>Francesco Barchi, Gianvito Urgese, Enrico Macii, and Andrea Acquaviva</i>	
Improved Test Solutions for COTS-Based Systems in Space Applications . . .	187
<i>Riccardo Cantoro, Sara Carbonara, Andrea Florida, Ernesto Sanchez, Matteo Sonza Reorda, and Jan-Gerd Mess</i>	

Analysis of Bridge Defects in STT-MRAM Cells Under Process Variations and a Robust DFT Technique for Their Detection 207
Victor Champac, Andres Gomez, Freddy Forero, and Kaushik Roy

Assessment of Low-Budget Targeted Cyberattacks Against Power Systems 232
XiaoRui Liu, Anastasis Keliris, Charalambos Konstantinou, Marios Sazos, and Michail Maniatakos

Efficient Hardware/Software Co-design for NTRU 257
Tim Fritzmann, Thomas Schamberger, Christoph Frisch, Konstantin Braun, Georg Maringer, and Johanna Sepúlveda

Author Index 281