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Evaluating the Impact of Resistive Defects on FinFET-Based SRAMs

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Abstract. The development of FinFET technology has made possible the continuous scaling-down of CMOS technological nodes. In parallel, the increasing need to store more information has resulted in the fact that Static Random Access Memories (SRAMs) occupy great part of Systems-on-Chip (SoCs). The manufacturing process variation has introduced several types of defects that directly affect the SRAM's reliability, causing different faults. Thus, it remains unknown if the fault models used in CMOS memory circuits are sufficiently accurate to represent the faulty behavior of FinFET-based memories. In this context, a study of manufacturing's functional implications regarding resistive defects in FinFET-based SRAMs is presented. In more detail, a complete analysis of static and dynamic fault behavior for FinFET-based SRAMs is described. The proposed analysis has been performed through SPICE simulations, adopting a compact Predictive Technology Model (PTM) of FinFET transistors, considering different technological nodes. Faults have been categorized as single or coupling, static or dynamic.

Keywords: FinFET, SRAM, Resistive Defects, SPICE, PTM.

1 Introduction

During the last decades, important advances in nano-scale technology have allowed to miniaturize and integrate hundred million transistors in a small silicon area. Since the development of the first commercial Integrated Circuit (IC), miniaturization and integration have been carried out following Moore's Law. Every two years, new circuits designed with smaller technological nodes were announced by the industry. However, significant changes to the paradigms of digital and analog circuit design were required throughout this technological progression of the Metal-Oxide Semiconductor Field Effect Transistors (MOSFETs) technology.

In technological nodes below 20nm, the gate terminal begins to lose control over the potential distribution and current flow of the transistor's channel region. This causes a

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phenomenon denominated Short-Channel Effect (SCE), which occurs due to the proximity between source and drain [1]. In the face of this adversity, new types of transistors have been designed to address the challenges caused by the scaling of CMOS transistors. Two technologies are widely adopted: Silicon-On-Insulator (SOI) MOSFET and FinFET. In fact, FinFET technology is already replacing CMOS transistors in state-of-the-art ICs – major electronics companies such as Intel [2] and Samsung [3] have already migrated to FinFET technology owing to its reduced short channel effects, electrostatic characteristics [4–6], and its compatibility with standard CMOS manufacturing process [7, 8].

As a result of this changes in technological paradigms caused by the introduction of the FinFET technology, several circuit devices needed to be redesigned, tested, and evaluated. One special kind of circuit that can be cited in this context are Static Random Access Memories (SRAM), the focus of this research. Due to the always-increasing need to store more and more information on chip, SRAMs have become the main contributor to the overall area of Systems-on-Chips (SoCs) [9]. Thus, the overall performance of the chip can be improved significantly by optimizing these memory circuits.

As explained in [10], SRAMs are designed with high density and produced at the limit of the technological process. Hence, they are very susceptible to manufacturing defects. The resistive defect model, which can be modeled as resistive-open or resistive-bridge, is a well-accepted defect model studied in bulk CMOS technology. A resistive-open defect is defined as a resistor between two circuit nodes that share a connection [11], while a resistive-bridge is defined as a resistor between two circuit nodes that should not be connected [12, 13]. Open defects have traditionally been a concern in the CMOS technology test scenario. More recently, this concern shifted towards weak resistive-open and weak resistive-bridge defects as their probability of occurrence may increase in nanometer technologies due to the ever-growing number of interconnections between layers [11].

While the influence of resistive defects in circuit parameters (e.g. voltage, current) is irrefutable, it is easier to evaluate their impact by analyzing what faulty behaviors they lead to. Functional faults are deviations from expected behavior of the memory under a set of operations [14]. Faults can be static (whose occurrence happens with one operation) and dynamic, in which at least two consecutive operations are required to sensitize the fault. These faults generally cause timing dependent faults, meaning that at least a 2-pattern sequence is necessary to sensitize them [15]. Moreover, the number of dynamic faults is directly correlated to the presence of weak resistive defects [16].

With the scaling down of technological nodes, weak resistive defects are likely to be one of the main reliability challenges in IC design [17]. This can be partially attributed to the difficulty of detecting these defects, and therefore the dynamic faults they cause. Indeed, open/resistive vias are the most common origin of test escapes in deep-submicron technologies [18]. Many of the standard March algorithms fail to detect dynamic faults [11, 19, 20] or present certain limitations by limiting the number of consecutive operations required to sensitize the fault by no more than two [21–23]. Recently, a new March test designed for FinFET-based memories was proposed in [24]. The authors formulated this new test algorithm based on reports from their previous works in which

they observed dynamic faults sensitized by up to eight consecutive read operations [25, 26].

Traditionally, characterization of fault behavior observed in defective SRAM cells has been performed following a well stablished methodology based on SPICE electrical simulations. Many works focused on evaluating the resistance in which a certain defect starts to sensitize faults. This resistance, known as critical resistance, is the threshold between a fault-free and faulty behavior [27]. Critical resistances of resistive-open defects were investigated in [11, 19, 28, 29] adopting technological nodes of 130nm down to 40nm, while critical resistances of resistive-bridge defects were investigated in [30, 31] adopting technological nodes of 90nm down to 40nm.

However, all these previous researches were conducted using planar CMOS technology. So far, little research has been conducted considering resistive defects in FinFET memories. In [26], the authors modeled resistive open and bridge defects taking into account the physical structure of 28nm FinFET devices aiming to observe possible unique faults of this technology. An analysis of faults in FinFET SRAM cells affected by resistive defects was presented in [32]. Simulations were carried out using a 20nm technology model. No further works have been proposed focusing on smaller nodes. This is especially worrisome since 14nm FinFET devices are currently in production [33, 34].

This work presents a study on the behavior of FinFET-based SRAM cells affected by resistive defects. In particular, this study intends to map and determine how manufacturing defects, specifically resistive-open and resistive-bridge defects, impact in the behavior of FinFET SRAM cells. Resistive defects with different magnitudes were injected in memory bitcells aiming to sensitize static and dynamic faults. The analysis was performed through electrical simulation using HSPICE™ software and adopting Predictive Technology Models (PTM) [35] of multi-gate transistors based on 20nm, 16nm, 14nm, 10nm, and 7nm bulk FinFET. These analyses demonstrated that smaller FinFET technologies will be more prone to weak resistive defects and therefore dynamic faults, proving the need for specific test methodologies for this unique technology.

The rest of the work is organized as follows. Section 2 explains the concepts related to the design of FinFET SRAMs and the set of fault models adopted in this work. Next, Section 3 describes the simulation setup and the set of resistive defects injected into the SRAM cells. Section 4 discusses the results obtained from simulations and compares the different technological nodes. Finally, Section 5 presents this work's final considerations.

2 Background

FinFET circuits have been adopted as a way to continue the scaling of ICs and fulfill the performance requirements established by the miniaturization-oriented goals of More Moore. Thus, it is of vital importance to understand the aspects of FinFET-based SRAM arrays and the faults related to this new technology in order to identify discrep-

ancies caused by resistive defects. In this Section, main characteristics of FinFET technology and FinFET SRAM design are discussed, followed by the background on the fault models associated to resistive-open and resistive-bridge defects.

2.1 FinFET Characteristics

FinFET transistors are quasi-planar, multi-gate devices consisting of vertical silicon islands, denominated "fins", with metal wrapped around the gate and placed on top of the oxide. The first fabricated structure alike FinFETs was the DELTA [36], a double-gate MOS transistor manufactured in 1989. Afterward, other transistor structures were proposed aiming to surpass the scalability limitations of the CMOS technology [7]. It is possible to design different FinFET structures based on the way the transistors are fabricated. In Silicon-On-Insulator (SOI) FinFETs, fins are built over Buried Oxide (BOX) and are isolated from the substrate. In Bulk FinFETs, the fin is connected directly to the substrate through the oxide layer, and a Shallow Trench Isolation (STI) of oxide is formed on the side.

FinFETs can also be classified based on their gate configuration. In Shorted-Gate (SG) FinFETs, all three sides of the gate are physically shorted in order to create a single terminal, allowing a higher on-current and lower off-current. In Independent-Gate (IG) FinFETs, the top part of the gate is etched in order to create two independent gate terminals. This offers the possibility of applying different signals in each terminal, enabling the modulation of V_{TH} of the front-gate by biasing the back-gate. However, this also implies in a certain area penalty due to the necessity of two separate gate contacts [37].

The fundamental design parameters of a FinFET transistor are its fin's height (H_{FIN}), its thickness (T_{FIN}), and channel length (L_g). Other parameters, such as Gate Oxide Thickness (T_{OX}), Gate Work Function, Body Doping, Source/Drain Doping, and Supply Voltage complete the typical parameters [38]. Fig. 1 depicts the architecture of a Bulk FinFET transistor and its main parameters. In this work, the bulk-FinFET technology is studied.

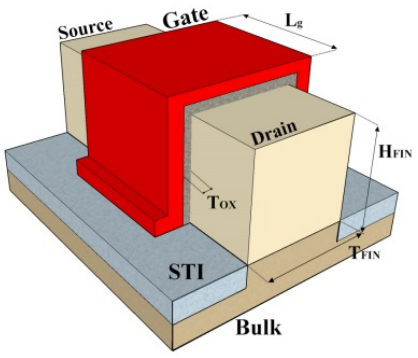

Fig. 1. Structure of bulk-FinFET transistors

The main advantage of this technology is to minimize the Short-Channel Effect (SCE), allowing the continuity of the downscaling of integrated circuits. This is possible due the improved control of gates over the conduction channel, bringing other benefits such as high density and low operational voltage.

2.2 Static Random Access Memories

A standard 6T SRAM cell is composed of six transistors; four of them form two cross-coupled inverters (M1 & M2, M3 & M4), while the other two act as Pass Gates (PG, M5 and M6), providing read and write access to the cell. The word line (*WL*) controls the two PG nMOS transistors that are each connected to their respective bit lines (*BL* and $\overline{BL}$). The value stored in the cell corresponds to the digital representation of the voltage on Q ('1' for V_{DD}, '0' for 0V). Fig. 2 shows a schematic of an 6T SRAM cell designed with SG-FinFET transistors.

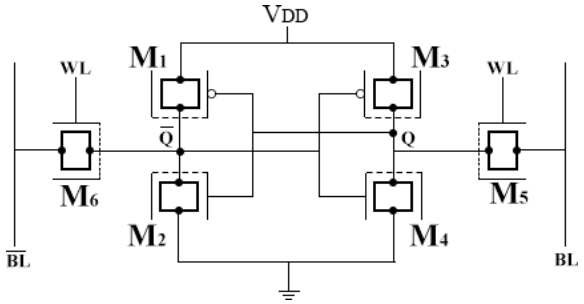

Fig. 2. FinFET-based SRAM-cell

Jointly, a group of SRAM cells forms a matrix structure, allowing data storage in any combination of rows and columns. All cells share electrical connections: vertically, through the bit line, and horizontally, through the word line. Each cell has a unique position (address), so it is possible to access each one of them individually by the appropriate selection of word and bit lines. Address decoders, write drivers, registers, and sense amplifiers complete the set of peripheral circuitry working to guarantee the proper operation of the memory. Fig. 3 depicts an example of this architecture. This structure is well known and a more detailed explanation can be found in literature.

Memories can operate in three distinct modes: hold mode, read mode, and write mode. In hold mode, no operations are being performed on the cell. The word line is off, and the cell has no connection with the rest of the memory array. In read mode, bit lines are pre-charged to V_{DD} and word line is turned on, enabling the cell to discharge BL or $\overline{BL}$ based on the stored value. During write mode, word lines are turned on and bit lines are kept in opposite voltage levels in order to force the new value into the cell.

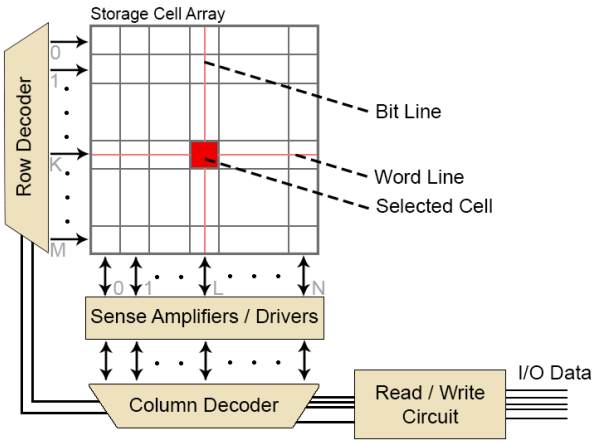

Fig. 3. Architecture of an SRAM memory.

2.3 FinFET SRAM

Technology scaling of conventional CMOS SRAMs are limited due to the random variations of threshold voltage (V_{TH}) caused by Random Dopant Fluctuation. As high doping is not required in FinFETs due to their enhanced SCE, Random Dopant Fluctuation is expressively reduced, which diminishes V_{TH} variations and allows V_{DD} to be scaled down. Furthermore, reduced Random Dopant Fluctuation also improves the Static Noise Margin (SNM) and consequently enhances the cell's robustness [8]. Moreover, improved sub-threshold swing allows not only lower V_{TH} for a given off-state leakage current, but also enhances the on-state current per device width. Such improvements shorten the read and write access times on SRAM cells. Thus, the FinFET technology can bring many specific advantages to SRAM memories' performance and stability.

The SRAM cell's structure is divided into three parts, with the proper notation of (PU:PG:PD) to describe its configuration, where PU, PG and PD stand for: Pull-Up, composed of the two pMOS transistors of the inverters; Pass Gate, consisting of the two pass-through nMOS transistors; and Pull-Down, which are the two nMOS transistors of the inverters, respectively. One of the drawbacks of designing SRAM cells with FinFET technology is the discrete nature of fins limited to a quantized number. Distinct configurations using different numbers of fins have been proposed for FinFET-based SRAM cell designs [39–41]. For this work, the High-Density configuration presented in [41] of (1:1:1) was adopted.

2.4 Fault Models Associated to Resistive Defects

Due to imperfections on the manufacturing process, memory cells may be affected by manufacturing defects such as resistive-open and/or resistive-bridge defects that can compromise the correct behavior of the device. These defects can be characterized as strong or weak defects based on the nature of the fault they sensitize: strong defects are

related to static faults, while weak defects are associated to dynamic faults. Faulty behaviors can be specified using Fault Primitive (FP), which characterizes the sensitizing sequence (*S*), the faulty behavior observed (*F*), and the output of read operations (*R*) [14, 23], following the notation <*S*/*F*/*R*>. A non-empty set of fault primitives is known as a Functional Fault Model (FFM). FPs can be classified as static or dynamic according to the number of required operations in order to sensitize the fault. Furthermore, the number of necessary operations to sensitize the fault may depend on many factors, such as defect resistance, operating temperature, process corner, among others [11].

Furthermore, an FP can also be classified by the number of cells involved: single-cell and multi-cell FP. In a single-cell FP, faulty behaviors are only observed in the defective cell. In multi-cell FP (also known as coupling-faults), two cells (or two groups of cells) interact to produce a fault. The cell that suffers the faulty behavior is the victim (v-cell), while the cell that triggers the fault is the aggressor (a-cell). It is important to note that the resistive defect can be present either in the a-cell and/or in the v-cell [14, 23].

Since an FFM is defined as a set of FPs, FFM will assume their characteristics, resulting in the follow classifications: static and dynamic FFM; single-cell and multi-cell FFM. In more details, FFMs can represent the following fault space that was considered in this work, and described in [12] and [14]:

- *Stuck-at Fault* (SAF): A cell is said to have a SAF (even know State Fault) when the cell is stuck and stores only one logic value '0' or '1';
- *No Store Fault* (NSF): This fault is the opposite to SAF, where a cell with NSF cannot retain any logic value in their nodes;
- *Transition Fault* (TF): A cell is said to have a TF if it fails to undergo a transition from '0' to '1' or vice versa when it is written;
- *Write Disturb Fault* (WDF): A cell is said to have a WDF if a non-transition write operation causes a transition in it;
- *Read Destructive Fault* (RDF): A cell is said to have an RDF if a read operation performed on the cell changes the data in the cell and returns the incorrect value to the output. This type of fault can also have a dynamic behavior classified as dRDF;
- *Deceptive Read Destructive Fault* (DRDF): A cell is said to have a DRDF if a read operation performed on the cell returns the correct logic value, but changes the contents of the cell. This type of fault can also have a dynamic behavior classified as dDRDF;
- *Incorrect Read Fault* (IRF): A cell is said to have an IRF if a read operation performed on the cell returns an incorrect logic value, even though the correct value is still stored in the cell. This type of fault can also have a dynamic behavior classified as dIFR;
- *Weak Read Fault* (WRF): A cell is said to have a WRF when, during the read operation, the sense amplifier cannot produce the correct logic output due to the small voltage difference between bit lines;
- *Disturb Coupling Fault* (CFds): This fault occurs in groups of at least two cells, called aggressor (a-cell) and victim (v-cell), and is sensitized when a read or write operation in an a-cell affects a v-cell or a group of v-cells, forcing them to change

their stored values. This type of fault can also have a dynamic behavior classified as dCFds;

- *Transition Coupling Fault* (CFtr): This fault occurs when a transition write operation performed on the v-cell fails due to a given logic value stored in the a-cell. Thus, the fault is sensitized by a write operation on the v-cell and setting the a-cell into a given state.
- *Read Disturb Coupling Fault* (CFrd): This fault occurs when a read operation performed on a v-cell changes the data in the cell and returns the incorrect value on the output if a given value is present in the a-cell. This type of fault can also have a dynamic behavior classified as dCFrd.
- *Incorrect Read Coupling Fault* (CFir): This fault occurs when a read operation performed on a v-cell returns an incorrect value on the output when a given value is present in the a-cell. This type of fault can also have a dynamic behavior classified as dCFir.

Table 1. Functional Fault Models and their respective Fault Primitives.

FFM	**FPs**
SAF	< 0/1/- >; < 1/0/- >
NSF	< 0/-/- >; < 1/-/- >
TF	< 0w1/0/- >; < 1w0/1/- >
WDF	< 0w0/1/- >; < 1w1/0/- >
RDF	< 0r0/1/1 >; < 1r1/0/0 >
dRDF	< 0w0r0/1/1 >; < 0w1r1/0/0 >; < 1w0r0/1/1 >; < 1w1r1/0/0 >
DRDF	< 0r0/1/0 >; < 1r1/0/1 >
dDRDF	< 0w0r0/1/0 >; < 0w1r1/0/1 >; < 1w0r0/1/0 >; < 1w1r1/0/1 >
IRF	< 0r0/0/1 >; < 1r1/1/0 >
dIRF	< 0w0r0/0/1 >; < 0w1r1/1/0 >; < 1w0r0/0/1 >; < 1w1r1/1/0 >
WRF	< 0r0/0/? >; < 1r1/1/? >
CFds	< x;0/1/- >; < x;1/0/- >
dCFds	< xx;0/1/- >; < xx;1/0/- >
CFtr	< x;0w1/0/- >; < x;1w0/1/- >
CFrd	< x;0r0/1/1 >; < x;1r1/0/0 >
dCFrd	< x;0w0r0/1/1 >; < x;0w1r1/0/0 >; < x;1w0r0/1/1 >; < x;1w1r1/0/0 >
CFir	< x;0r0/1/0 >; < x;1r1/0/1 >
dCFir	< x;0w0r0/1/0 >; < x;0w1r1/0/1 >; < x;1w0r0/1/0 >; < x;1w1r1/0/1 >

Table 1 shows the FFMs observed in this work and their respective FPs. As previously mentioned, an FFM is composed by a set of FPs represented by <*S*/*F*/*R*>. On

single-cell faults, *S* may assume none or one operation of read or write for a static FFM, and two or more operations for dynamic FFM.

For simplification purposes, FPs of dynamic FFMs are represented with only two operations. *F* represents the faulty behavior of the cell, and is represented by a logic '1' or '0'. *R* is the output of a read operation, represented by a logic '0' or '1'. In case no read operation is performed, '-' is adopted, while '?' is used when it is not possible to determine the output value. For coupling faults, *S* assumes the form of *x;y*, in which *x* is the operation in the a-cell and *y* is for v-cell. Furthermore, *xx* is used to represent a dynamic behavior of more than one operation. It's important to note that in this work, dynamic FPs are comprised of a write operation followed by consecutive *n* read operations. Thus, it's necessary to repeatedly read a cell and evaluate the retrieved value [14] .

3 Simulation Setup

In order to provide the proposed analysis, electrical simulations have been performed on HSPICE adopting a FinFET SRAM block composed of 1024 lines and 1024 columns each, connected to functional blocks, using a 20nm low-power PTM compact model and considering temperatures of -40ºC, 27ºC, and 125ºC. Furthermore, this work analyzes the impact of resistive defects on SRAM blocks designed in smaller technological nodes, such as 16nm, 14nm, 10nm, and 7nm. Table 2 presents the supply voltage adopted for each node. The operational clock signal frequency chosen is set to 1GHz. In order to simplify and fasten the simulations, only 8 lines consisting of 8 columns each were implemented, while the remaining cells were emulated by capacitances.

Table 2. Supply voltage of the analysed technological nodes.

Technological Node	V_{DD}
20nm	0.90V
16nm	0.85V
14nm	0.80V
10nm	0.75V
7nm	0.70V

To recreate an SRAM block as genuine as possible, auxiliary circuitry was used. A differential sense amplifier was adopted for read operations, while write operations were assisted by write buffers. Pre-charge circuits, row-decoders, and registers complete the setup. All circuits, including memory cells, were designed using the low power technological library. As stated before, the SRAM cell was designed using only one fin in each transistor to achieve higher densities.

3.1 Modeled Defects

In this work, a set of 12 defects was modeled and injected into a memory cell, one at a time. Six of them are classic resistive-open defects, previously studied for bulk CMOS technology [15]. In summary, resistive-open defects are non-designed resistances between two nodes that have a connection. Fig. 4 depicts the scheme adopted to model the resistive-open defects.

The other six defects analyzed are considered resistive-bridge defects, which are resistive connections between nodes that, upon design, were not connected [11]. Fig. 5 shows the set of resistive-bridge defects analyzed in this work. DFB1-DFB5 are classic resistive-bridge defects that have been previously analyzed in CMOS technology [12]. DFB6 is a new defect that, considering FinFET architecture, may create a bridge between drain and source of transistors [42]. Due to cell's symmetry, only one instance of each defect is necessary to analyze their impact on the cell's behavior.

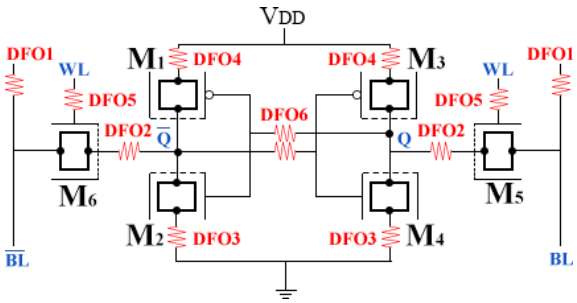

Fig. 4. Resistive-open defects injected into a SRAM cell.

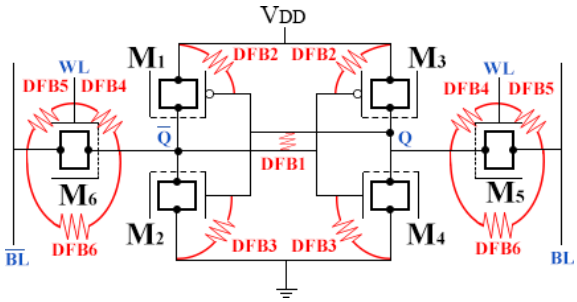

Fig. 5. Resistive defects injected into a SRAM cell.

3.2 Evaluation of Defect Size on Fault Behavior

To analyze the impact of each defect on the behavior of memory cells, an automated tool was developed. For each defect, simulations were performed while varying the resistance value of modeled defects up to a maximum of 20MΩ, or until the occurrence of a static fault. The resistance on this iteration is defined as "upper limit" and, based on this resistance value, the tool simulated the circuit again using increasingly weaker resistances in order to observe either dynamic faults or fault-free behavior.

Applying this procedure, it is possible to observe three distinct cases: the defect is too weak to sensitize any type of fault at logic level; the defect is weak, but great enough to sensitize dynamic faults; and the defect is great enough to sensitize static faults. The output of read operations and internal nodes of the cell are analyzed in order to identify faults.

To evaluate defects that result in single static faults, simple verification of the value is performed after the defect is injected. Single write and read operations ($0r0$, $1r1$, $0w0$, $0w1$, $1w0$ and $1w1$) are executed to analyze static faults. To evaluate dynamic faults, a write followed by n read operations were performed ($0w0r0^n$, $0w1r1^n$, $1w0r0^n$ and $1w1r1^n$, where n is number of operations). Note that n was defined to be at maximum 50 read operations. The analysis for coupling faults is similar, with the exception that for this type of fault, operations may be performed in certain cells, while evaluation is performed in a different cell or group of cells in the array.

4 Results

This Section summarizes the results and discusses the relation between defect size and cell behavior. First, results obtained for resistive-open defects and resistive-bridge defects considering the 20nm node in a nominal temperature of 27°C are presented. Next, an evaluation comparing the behavior of this same node in temperatures of -40°C and 125°C is presented. These analyses were first presented in [32], and are further extended in this work by repeating the same experiment using smaller technological nodes. In all analyses, the obtained results are the fault observed and the critical resistance.

4.1 Resistive-Open Defects

Results for resistive-open defects are shown in Fig. 6, which illustrates the relation between defect size and faults observed on affected cells at room temperature (27ºC). For DFO4, within the specified range of 0-20MΩ no faults were observed at 27°C. Observing the remaining defects, it is possible to conclude that DFO1 is the most critical one; it demonstrates a fault free interval of only 15.3kΩ. Dynamic behaviors were only reported for DFO2 and DFO3. It is possible to summarize the results: TFs can be observed for defects DFO1, DFO5, and DFO6. RDF and dRDF can be observed injecting RODF3. Finally, DRDF and dDRDF are observed when injecting DFO2 and DFO3.

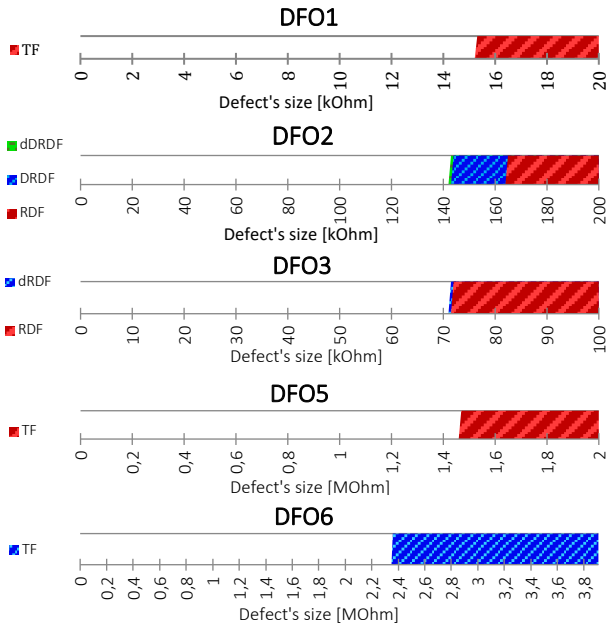

Fig. 6. Faults observed during simulations of SRAM cells affected by resistive-open defects of different magnitudes.

4.2 Resistive-Bridge Defects

As previously mentioned, resistive-bridge defects create connections between nodes that were not planned upon design. Therefore, depending on the defect size, such defects may actively unbalance the cell and cause faults such as NSF and SAF. The full relation between defect size and observed faults is depicted in Fig. 7. From the obtained results, it is possible to conclude that the most critical resistive-bridge defect is DFB3 as it creates the greatest faulty behavior interval (from 0 to 46kΩ).

However, there is a different aspect of resistive-bridge defects the results draw special attention to: as such defects create connections, a resistive-bridge defect affecting one cell may have an impact in other fault-free neighbor cells, causing Coupling Faults (CF). In Fig. 7, this was defined as “Array Impact”, and observed in DFB5 and DFB6. It is important to mention that these “Array Impact” faults affected fault-free cells. Fig. 8 depicts this behavior. It shows the simulation of a cell that is located at row 0 and is affected by a resistive-bridge defect (DFB5) that creates a connection between the word line 0 (WL0) and $\overline{BL}$ of magnitude 11.5 kΩ. This defect size does not sensitize any fault in a-cell, as shown in Fig. 7. A write ‘0’ operation is successfully performed on the cell, followed by three consecutive read operations in the same cell on row 0. The faulty behavior is observed in a v-cell in row 1, as a dynamic CFrd, and in a v-cell in row 2 as a CFrd.

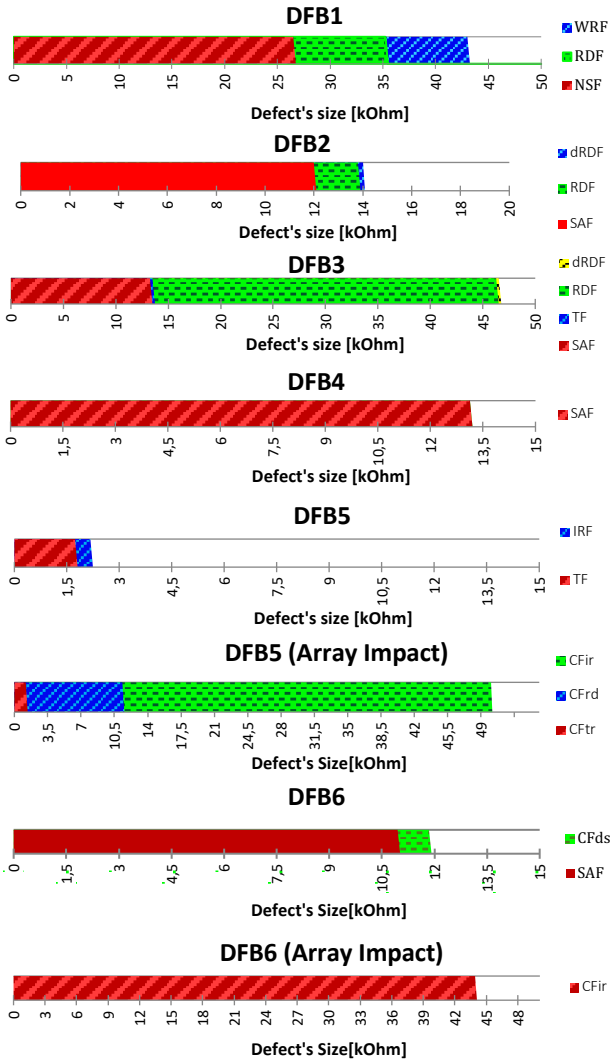

Fig. 7. Faults observed during simulations of SRAM cells affected by resistive-bridge defects of different magnitudes.

By performing a read operation on row 1 (Fig. 8), $\overline{\text{BL}}$ is not able to charge as it is being drained by the WL0. This results in an IRF, as can be seen in the *Out* signal. As all of the three analyzed cells are located on the same column, they all share the same output signal. A subsequent read operation has a bigger impact, causing a dynamic CFrd on the cell. The same destructive behavior is observed when performing subsequently read operations in another fault-free cell from a different row, this time a static CFrd can be observed.

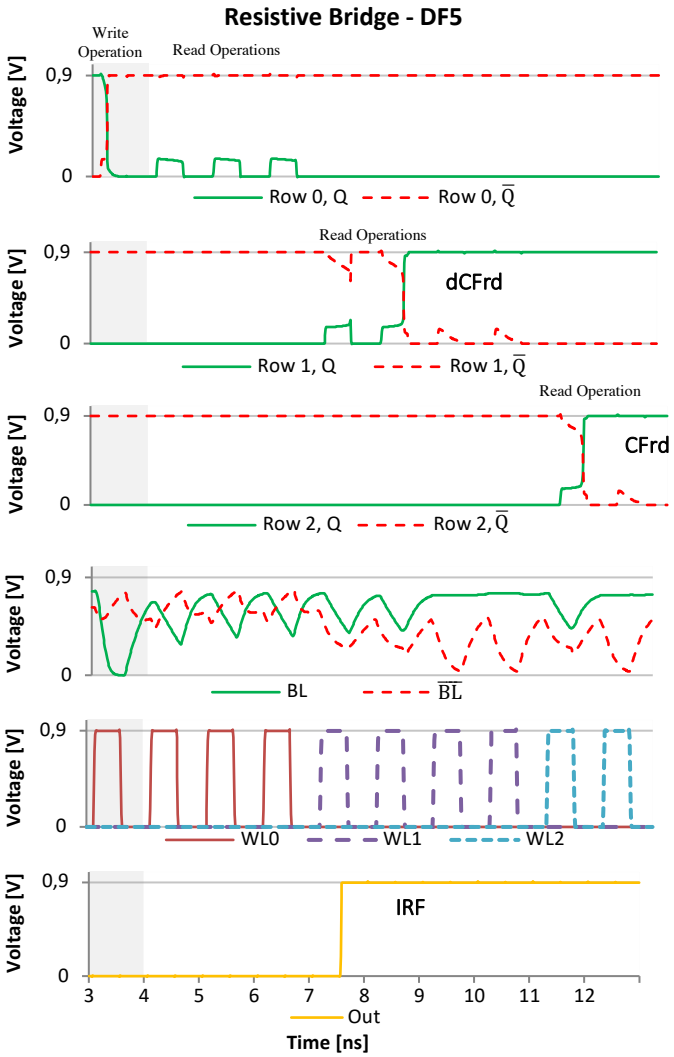

Fig. 8. Simulation output of a cell affected by a resistive-bridge causing faults on other cells of the array.

Additionally, operations performed on fault-free cells can affect defective cells as long as they are in the same column. This way, the fault-free cell is the aggressor and the faulty cell is the victim. Fig. 9 illustrates this fault behavior on a cell affected by DFB6, which creates a resistive-bridge between source and drain of transistor M5, connecting $\overline{BL}$ and $\overline{Q}$. As the fault-free cell on row 2 is written, the value on the defective cell on row 1 is flipped. This happens due to the shared connection between $\overline{BL}$ and $\overline{Q}$. As $\overline{BL}$ is discharged due to a write '0' operation, $\overline{Q}$ discharges as well, causing a misbalancing, and eventually a flip on the stored value. This can also be considered as a

"following-signal" behavior, as $\overline{Q}$ follows the value on $\overline{BL}$. The same behavior is observed on cells affected by DFB4, as the affected node is now connected to WL.

Fig. 10 depicts this particular behavior. It shows the simulation of a cell affected by a DFB4 of magnitude 13kΩ. In Fig. 7, this behavior is classified as SAF. This defect creates a connection between $\overline{Q}$ and WL. This way, $\overline{Q}$ follows the voltage on WL, causing an inconsistent behavior that may not be trivial to detect. The behavior observed resembles an SAF as the cell can only store '1' while the word line is off.

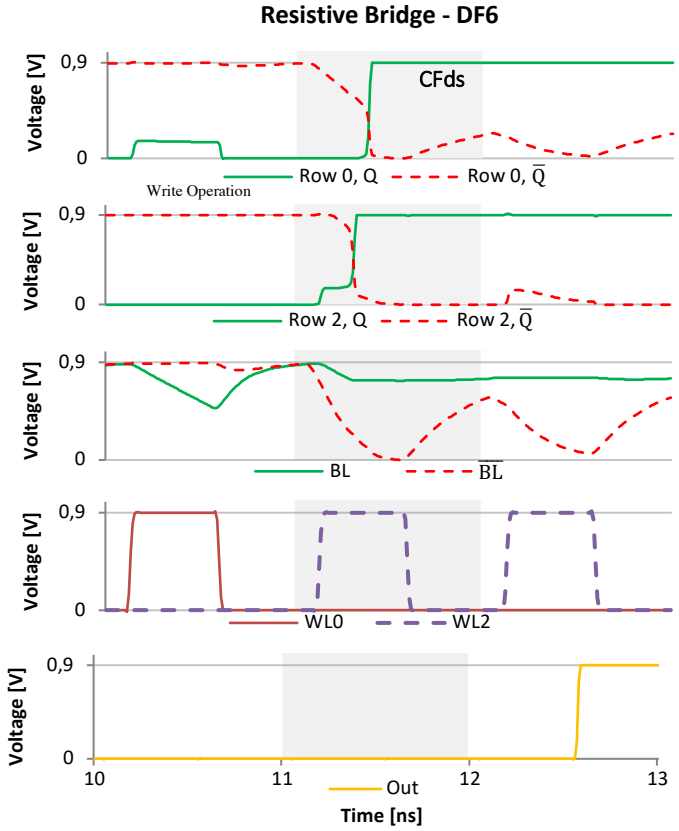

Fig. 9. Simulation output of a cell affected by a resistive-bridge defect suffering a destruction fault caused by an operation in a neighbor cell.

4.3 Analysis considering different operating temperatures

Table 3 shows the comparison between the critical resistances for resistive-open and resistive-bridge defects considering three different temperatures, -40°C, 27°C, and 127°C. Analyzing the results obtained throughout simulations, it is possible to observe that for each defect, a similar relation between critical resistances and temperature exists. In DFO1, DFO2, DFO3, DFO4, DFO6, DFB2, and DFB5 (register) an increased

temperature worsens the critical resistance. On the contrary, DFO5, DFB1, DFB3, DFB4, DFB5 (cell and array) and DFB6 are more prominent in lower temperatures.

The operating temperature affects the critical resistances, since the current capabilities of the transistors are also affected. In this manner, the process of charging and discharging the nodes and the resistive-open and bridge defect's value are affected by temperature.

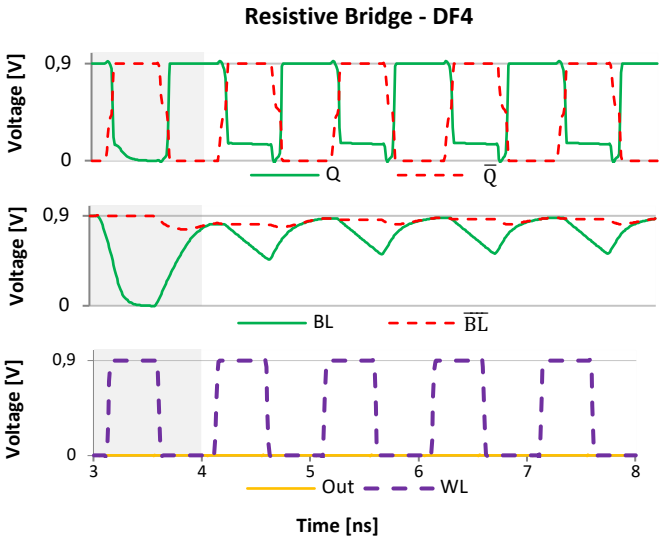

Fig. 10. Simulation output of a cell affected by a resistive-bridge defect connecting $\overline{Q}$ to the word line.

On the one hand, for resistive-open defects, the high temperature facilitates the occurrence of faults, because it lowers the critical resistance. However, for DFO5, low resistance slightly moved the cell's operational window to a more convenient period within higher temperatures, resulting in an improvement of operation in this design. Further, it is interesting to note, that DF4 only causes faults at the highest temperature setting.

On the other hand, resistive-bridge defects are more likely to sensitize faults considering lower temperature. Note that the critical resistance value necessary to cause RDFs decreases with temperature for DFB2 and DFB3, because the resistance alters the discharge characteristics of nodes. Note that for resistive-bridge defects a smaller resistance value represents a stronger defect. Considering DFB5, it is possible to observe that the TF occurs with a smaller resistance value when simulating the memory cell operating at -40ºC. Finally, coupling faults are more prominent in low temperature, since a weaker defect is necessary to cause the fault.

The presented analysis considering different operating temperatures demonstrates a pattern for FinFET-based SRAMs and will further assist in future researches on evaluating weak resistive defects' impact on memory cells.

Table 3. Critical Resistance Values for Different Temperatures.

DF	Temperature		
	-40°C	***27°C***	***125°C***
DFO1	16.9kΩ (TF)	15.3kΩ (TF)	13.6kΩ (TF)
DFO2	297kΩ (dDRDF)	144kΩ (dDRDF)	73kΩ (dRDF)
DFO3	137kΩ (dRDF)	71.5kΩ (dRDF)	37.2kΩ (dRDF)
DFO4	-	-	6.6MΩ (dRDF)
DFO5	1.4MΩ (TF)	1.47MΩ (TF)	1.6MΩ (TF)
DFO6	2.58MΩ (TF)	2.46MΩ (TF)	2.23MΩ (TF)
DFB1	54.4kΩ (WRF)	41.6kΩ (WRF)	30.8kΩ (WRF)
DFB2	13.9kΩ (dRDF)	13.8kΩ (dRDF)	14.8kΩ (dRDF)
DFB3	54.6kΩ (dRDF)	46.4kΩ (dRDF)	37.8kΩ (dRDF)
DFB4	14.1kΩ (dRDF)	13.2kΩ (dRDF)	12.8kΩ (dRDF)
DFB5	1.74kΩ (TF) 57.5kΩ (dCFir)	2.13kΩ (IRF) 49.5kΩ (dCFir)	3.53 kΩ (IRF) 38.2kΩ (dCFir)
DFB6	11.61kΩ (SAF) 52.6kΩ (dCFir)	10.92kΩ (SAF) 44.0kΩ (dCFir)	10.52kΩ (SAF) 32.0kΩ (dCFir)

4.4 Analysis considering different nodes

In order to evaluate critical resistances for smaller nodes, an extensive fault mapping process was carried out, adopting different technological nodes: 16nm, 14nm, 10nm, and 7nm. Table 4 to 9 present the faults observed in each simulation setup, including the 20nm node as reference. The resistance values shown represent the critical resistance responsible to sensitize a fault at logic level.

The tables are grouped in two sets according to the kind of defect. In the first set, the critical resistance associated to resistive-open defects is analyzed considering three different operating temperatures. The second set presents the results for bridge defects. Table 4 presents the results obtained for resistive-open defects considering the temperature of 27ºC. Analyzing the summarized results, it is possible to observe a significant change in critical resistance for the same defect in different technological nodes. The only exception is DFO1, whose critical resistance remained around 14kΩ. Note that with DFO4 no faults have been observed for the considered temperature range. For all other resistive-open defects, the scale-down of technological nodes made them less relevant as only stronger defects are now necessary to sensitize faults. In fact, the critical resistance for DFO2 in a 20nm node is more than 30 times smaller when compared to its critical resistance in 7nm technology.

Table 4. Critical Resistances for resistive-open defects at 27°C.

Defect	Fault	Critical Resistance [kΩ]				
		20nm	**16nm**	**14nm**	**10nm**	**7nm**
DFO1	TF	15.3	13.8	12.2	13.7	16.6
DFO2	DRDF	144.3	225.2	463.9	937.4	4500.0
	RDF	165.4	232.2	505.4	-	-
	dDRDF	144.2	224.5	461.0	923.8	4041.2
DFO3	RDF	71.6	103.4	190.1	357.9	1345.9
	dRDF	71.5	103.3	189.5	356.3	1324.8
DFO5	TF	1471.1	1858.0	2385.6	2778.4	3137.5
DFO6	TF	2457.5	3665.9	5105.0	6055.0	7685.0

A similar behavior can be observed in the results shown in Tables 5 and 6, which present the results obtained for the simulations injecting resistive-open defects with operating temperature set to 125ºC and -40ºC, respectively. Once again, all defects presented a significant increase in critical resistance, except for DFO1. Note also that DFO4 only caused faults when considering a temperature of 125ºC and the range of resistance used in the executed simulations.

Table 5. Critical Resistances for resistive-open defects at 125°C.

Defect	Fault	Critical Resistance [kΩ]				
		20nm	**16nm**	**14nm**	**10nm**	**7nm**
DFO1	TF	13.6	11.5	9.5	10.1	11.2
DFO2	RDF	73.1	93.0	137.7	206.3	420.3
	dRDF	73.0	92.8	137.4	205.9	420.0
DFO3	RDF	37.3	46.2	64.9	92.8	182.3
	dRDF	37.2	46.1	64.8	92.7	182.1
DFO4	dDRDF	6598.7	17662.9	-	-	-
DFO5	TF	1566.9	1947.0	2440.5	2851.4	3145.8
DFO6	TF	2231.5	3384.4	4671.6	5485.2	6225.0

Table 6. Critical Resistances for resistive-open defects at -40°C.

Defect	Fault	Critical Resistance [kΩ]				
		20nm	**16nm**	**14nm**	**10nm**	**7nm**
DFO1	TF	16.9	16.0	14.9	17.4	21.7
DFO2	DRDF	297.4	694.6	-	-	-
	dDRDF	296.7	680.2	7414.0	-	-
DFO3	RDF	136.7	261.3	1301.3	-	-
	dRDF	136.6	260.4	1285.0	9187.6	-
DFO5	TF	1393.5	1764.7	2278.1	2713.3	3060.8
DFO6	TF	2575.3	3830.4	5345.0	6360.0	7985.0

In Tables 7, 8, and 9, the results obtained from the analysis of faults caused by resistive-bridge defects in the temperatures of 27°C, 125°C and -40°C are shown, respectively. Analyzing the results obtained in Table 7, it is possible to observe a significant change in critical resistance (increasing 84%) for the defect DFB1, when moving from 20nm to 7nm technology. Reducing the technology node also causes some variation to the value of critical resistance for the remaining defects. The lowest values tend to appear for the 14nm technology, while for 7nm the value increases when compared to any other technology node simulated.

It is important to mention that some faults are masked by others. This happens to TF in DFB1, which is masked by NSF and SAF. This also occurs with WRF in DFB2 and DFB3. In older technologies, a well-defined range for such behavior is encountered, while FinFET's technology range of transitions is comparably diffuse, since the critical resistance values often differ by less than 1kΩ. There are presented some faults with the same value, because this faults are noted for some nodes, but are masked for another. For example, in DFB1 for the 7nm technology, WRF and RDF are masked by NSF.

Observing some faults, the SAF can be notice that the value stuck-at could be different, according how the resistance is presented in the cell. For example, in defect DFB2, SAF is stuck-at '1', however this would be '0' if the resistance are connected to $\overline{Q}$. Fr the CFir array faults of DFB5 and DFB6, the value of critical resistance keep the higher in all cases; this event occurs due the variations in the register's sensibility in the set of V_{DD} and frequency operation used.

Table 7. Critical Resistance Values for DFB at 27°C.

Defect	Fault		Critical Resistance [kΩ]				
			20nm	**16nm**	**14nm**	**10nm**	**7nm**
DFB1	NSF		26.67	32.93	49.14	58.70	75.78
	WRF		43.11	45.38	49.14	58.70	75.78
	RDF		35.21	37.85	49.14	58.70	75.78
	dRDF		35.39	43.73	50.04	59.80	76.88
DFB2	SAF1		11.98	11.09	10.58	11.38	13.40
	TF		11.98	11.09	10.60	11.42	13.92
	RDF		13.80	12.18	11.36	12.34	14.40
	dRDF		14.04	12.20	11.44	14.62	15.56
DFB3	SAF0		13.22	12.82	12.56	12.55	15.04
	TF		13.46	13.42	13.10	13.14	17.60
	RDF		46.41	45.48	45.42	53.03	66.92
	dRDF		46.42	45.49	45.44	53.04	67.00
DFB4	SAF0		13.20	12.32	11.54	12.56	15.02
	RDF		13.20	12.82	12.64	13.80	16.26
DFB5	Cell	TF	1.65	1.66	1.36	1.37	2.29
		IRF	2.12	2.02	1.24	1.26	2.34
	Array	CFtr	1.67	1.67	1.36	1.37	2.32
		CFrd	11.36	10.68	9.40	10.34	12.24
		CFir	50.19	26.31	24.29	27.50	38.98
		dCFrd	11.92	10.86	9.61	10.66	12.36
		dCFir	50.20	10.87	24.40	27.66	39.01
DFB6	Cell	SAF0	10.92	10.02	9.67	10.26	11.16
	Array	CFds	11.86	10.02	9.67	10.26	11.16
		CFir	44.00	22.83	20.81	24.02	35.50
		dCFir	44.01	22.88	20.88	24.12	35.65

Table 8. Critical Resistance Values for DFB at 125°C.

Defect	Fault		Critical Resistance [kΩ]				
			20nm	**16nm**	**14nm**	**10nm**	**7nm**
DFB1	NSF		18.70	18.52	20.16	27.27	43.88
	WRF		32.09	29.55	30.31	35.69	44.06
	RDF		21.88	20.04	21.26	27.63	43.80
	dRDF		21.97	20.14	21.36	28.07	44.06
DFB2	SAF1		11.60	10.12	9.21	9.61	10.78
	TF		11.60	10.12	9.21	9.61	10.80
	RDF		14.78	12.14	10.44	10.56	11.50
	dRDF		14.95	12.20	10.68	10.68	11.60
DFB3	SAF0		12.86	11.20	9.88	10.38	11.80
	TF		12.86	12.22	9.96	10.42	12.84
	RDF		37.81	34.63	32.66	36.25	42.77
	dRDF		37.82	34.64	32.68	36.26	42.79
DFB4	SAF0		12.84	11.18	9.86	10.36	11.80
	RDF		12.84	11.18	10.22	10.36	12.16
	dRDF		12.85	11.19	10.41	10.53	12.17
DFB5	Cell	TF	1.57	157	1.24	1.20	2.00
		IRF	3.48	3.54	2.77	2.83	3.06
	Array	CFtr	1.57	1.57	1.24	1.21	2.02
		CFrd	10.74	9.19	7.60	8.11	9.20
		CFir	38.74	16.12	14.96	17.76	23.36
		dCFrd	10.78	9.21	7.67	8.19	9.25
DFB6	Cell	SAF0	10.52	9.09	8.44	8.84	9.55
	Array	CFir	10.52	9.09	8.44	8.84	9.56
		dCFir	31.99	12.25	11.09	13.89	19.49

Analyzing the data of Table 8 and 9, it is observed that the effect of temperature variation is more prominent in the 7nm node, whose the critical resistance in Table 8 is lower than the 20nm node. However, in Table 9 the situation is inversed and the critical resistance of the 7nm node is higher. It may be noted that the dynamic fault occurrence rate is higher when compared to open defects for all nodes.

Table 9. Critical Resistance Values for DFB at -40°C.

Defect	Fault		Critical Resistance [kΩ]				
			20nm	**16nm**	**14nm**	**10nm**	**7nm**
DFB1	NSF		47.35	60.60	66.90	83.08	113.81
	WRF		55.74	60.60	66.91	83.08	113.81
	RDF		55.05	60.60	66.90	83.08	113.81
	dRDF		56.14	61.02	67.12	85.45	114.74
DFB2	SAF1		12.76	12.34	12.20	13.38	16.22
	TF		12.76	12.40	12.46	13.92	18.48
	RDF		13.86	12.92	12.44	13.38	16.28
	dRDF		14.04	13.73	14.03	16.17	20.14
DFB3	SAF0		14.08	13.78	13.56	15.20	18.92
	TF		14.99	15.34	14.02	15.70	22.96
	RDF		54.62	55.99	58.51	71.21	96.33
	dRDF		54.63	56.00	58.52	71.29	97.02
DFB4	SAF0		14.06	13.76	13.54	15.20	18.92
	RDF		14.08	13.76	13.54	15.20	18.92
DFB5	Cell	TF	1.74	1.84	1.51	1.55	2.89
		IRF	0.64	0.58	0.81	0.87	3.16
		dRDF	0.65	1.81	1.52	1.58	2.66
	Array	CFtr	1.74	1.84	1.52	1.54	2.85
		CFrd	11.88	12.04	11.12	12.64	15.44
		CFir	57.61	33.07	31.38	38.05	49.53
		dCFrd	13.12	12.05	11.44	12.65	15.82
		dCFir	57.62	33.08	31.39	38.06	49.54
FB6	Cell	SAF0	11.62	11.00	10.60	10.96	12.96
	Array	CFds	12.86	12.92	12.86	14.30	12.96
		CFir	52.58	28.04	24.25	30.92	42.40
		dCFir	52.59	28.06	24.27	30.94	42.42

5 Final Remarks

This work presents an analysis of the behavior of FinFET-based SRAMs affected by resistive defects. The range of analyzed defects is vast and includes weak resistive-open and weak resistive-bridge defects that may escape manufacturing tests. Faulty behaviors detected by an automated tool were mapped and categorized in different kinds of faults. Further, the impact of defects on other cells of the array was evaluated, showing that defects that do not sensitize faults in the defective cell may still compromise the behavior of other cells. The fault models categorized comprise single and couple, static and dynamic faults. Finally, each defect was further characterized considering three

different operating temperatures (-40°C, 27°C, and 125°C) and five technological nodes (20nm, 16nm, 14nm, 10nm, and 7nm). Except for DFO5, increasing the temperature amplify the impact of resistive-open defects on memory cells. Moreover, a significant increase in critical resistance was observed when mapping faults in smaller technologies, especially for DFO4. Thus, it is possible to conclude that only stronger defects will sensitize faults in further scaled memories.

As for resistive-bridge defects, each defect showed a particular behavior when considering different operating temperatures, mainly the 7nm that suffers great variations for temperature variation. Besides some exceptions, lower temperatures increase the critical resistance. Coupling faults were observed in cells affected by DFB5 and DFB6.

Dynamic faults will increase their range of appearance with the reduction of technology, to the open defects consequently the 7nm technology presents a high dynamic fault rate. Considering bridge defect the occurrence of dynamic faults is variable. It is important to mention that weak defects, that do not cause any faulty behavior, may become a reliability concern over lifetime. Under these circumstances, the necessity to adopt defect-oriented test methodologies for performing the manufacturing test procedures increases.

It is important to highlight that weak defects, that do not cause any faulty behavior, may become a reliability concern over lifetime. Under these circumstances, the necessity to adopt defect-oriented test methodologies for performing the manufacturing test procedures increases.

Finally, with this mapping and characterization of different resistive defects, it is possible to start analyzing the impact of these defects when considering memory block's in combination with other reliability issues, such as aging and/or noise tolerance.

References

1. Colinge, J.-P.: FinFETs and Other Multi-Gate Transistors. Springer US, Boston, MA (2008).
2. Intel: Intel® 22 nm Technology, http://www.intel.com/content/www/us/en/silicon-innovations/intel-22nm-technology.html.
3. Samsung: Strong 14nm FinFET Logic Process and Design Infrastructure for Advanced Mobile SOC Applications. (2013).
4. Tang, S.H., Chang, L., Lindert, N., Yang-Kyu Choi, Wen-Chin Lee, Xuejue Huang, Subramanian, V., Bokor, J., Tsu-Jae King, Chenming Hu: FinFET-a quasi-planar double-gate MOSFET. In: 2001 IEEE International Solid-State Circuits Conference. Digest of Technical Papers. ISSCC (Cat. No.01CH37177). p. 118–119,. IEEE (2001).
5. Bin Yu, Leland Chang, Ahmed, S., Haihong Wang, Bell, S., Chih-Yuh Yang, Tabery, C., Chau Ho, Qi Xiang, Tsu-Jae King, Bokor, J., Chenming Hu, Ming-Ren Lin, Kyser, D.: FinFET scaling to 10 nm gate length. In: Digest. International Electron Devices Meeting,. pp. 251–254. IEEE (2002).
6. Chang, J.B., Guillorn, M., Solomon, P.M., Lin, C.-H., Engelmann, S.U., Pyzyna, A., Ott, J.A., Haensch, W.E.: Scaling of SOI FinFETs down to fin width of 4 nm for the 10nm technology node. In: 2011 Symposium on VLSI Technology - Digest of Technical Papers (2011).
7. Colinge, J.P., Chandrakasan, A.: FinFETs and other multi-gate transistors. (2008).

8. Bhattacharya, D., Jha, N.K.: FinFETs: From Devices to Architectures. Adv. Electron. 2014, 1–21 (2014).
9. International Technology Roadmap for Semiconductors: Executive Summary - 2013 Edition. (2013).
10. Bosio, A., Dilillo, L., Girard, P., Pravossoudovitch, S., Virazel, A.: Advanced test methods for SRAMs. Proc. IEEE VLSI Test Symp. 300–301 (2012).
11. Dilillo, L., Girard, P., Pravossoudovitch, S., Virazel, A., Borri, S., Hage-Hassan, M.: Resistive-Open Defects in Embedded-SRAM Core Cells: Analysis and March Test Solution. 13th Asian Test Symp. 266–271 (2004).
12. Fonseca, R.A., Dilillo, L., Bosio, A., Girard, P., Pravossoudovitch, S., Virazel, A., Badereddine, N.: Analysis of resistive-bridging defects in SRAM core-cells: A comparative study from 90nm down to 40nm technology nodes. 2010 15th IEEE Eur. Test Symp. ETS'10. 1, 132–137 (2010).
13. Li, J.C.M., Chao-Wen Tseng, McCluskey, E.J.: Testing for resistive opens and stuck opens. In: Proceedings International Test Conference 2001 (Cat. No.01CH37260). pp. 1049–1058. IEEE (2001).
14. Van de Goor, A.J., Al-Ars, Z.: Functional memory faults: a formal notation and a taxonomy. Proc. 18th IEEE VLSI Test Symp. 281–289 (2000).
15. Borri, S., Hage-Hassan, M., Dilillo, L., Girard, P., Pravossoudovitch, S., Virazel, A.: Analysis of Dynamic Faults in Embedded-SRAMs: Implications for Memory Test. J. Electron. Test. 21, 169–179 (2005).
16. Dubey, P., Garg, A., Mahajan, S.: Study of Read Recovery Dynamic Faults in 6T SRAMS and Method to Improve Test Time. J. Electron. Test. 26, 659–666 (2010).
17. Harutyunyan, G., Shoukourian, S., Vardanian, V., Zorian, Y.: Impact of process variations on read failures in SRAMs. In: East-West Design & Test Symposium (EWDTS 2013). pp. 1–4. IEEE (2013).
18. Needham, W., Prunty, C., Eng Hong Yeoh: High volume microprocessor test escapes, an analysis of defects our tests are missing. In: Proceedings International Test Conference 1998 (IEEE Cat. No.98CH36270). pp. 25–34. Int. Test Conference (1998).
19. Borri, S., Hage-Hassan, M., Dilillo, L., Girard, P., Pravossoudovitch, S., Virazel, A.: Analysis of dynamic faults in embedded-SRAMs: Implications for memory test. J. Electron. Test. Theory Appl. 21, 169–179 (2005).
20. Dubey, P., Garg, A., Mahajan, S.: Study of Read Recovery Dynamic Faults in 6T SRAMS and Method to Improve Test Time. J. Electron. Test. 26, 659–666 (2010).
21. Benso, A., Bosio, A., Di Carlo, S., Di Natale, G., Prinetto, P.: March AB, March AB1: New March Tests for unlinked dynamic memory faults. Proc. - Int. Test Conf. 2005, 834–841 (2005).
22. Bosio, A., Di Carlo, S., Di Natale, G., Prinetto, P.: March AB, a state-of-the-art march test for realistic static linked faults and dynamic faults in SRAMs. IET Comput. Digit. Tech. 1, 237–245 (2007).
23. Hamdioui, S., Al-Ars, Z., Van De Goor, A.J.: Testing static and dynamic faults in random access memories. Proc. IEEE VLSI Test Symp. 2002–Janua, 395–400 (2002).
24. Harutyunyan, G., Martirosyan, S., Shoukourian, S., Zorian, Y.: Memory Physical Aware Multi-Level Fault Diagnosis Flow. IEEE Trans. Emerg. Top. Comput. 1–1 (2018).
25. Harutyunyan, G., Tshagharyan, G., Zorian, Y.: Test and Repair Methodology for FinFET-Based Memories. IEEE Trans. Device Mater. Reliab. 15, 3–9 (2015).
26. Harutyunyan, G., Tshagharyan, G., Vardanian, V., Zorian, Y.: Fault modeling and test algorithm creation strategy for FinFET-based memories. In: 2014 IEEE 32nd VLSI Test Symposium (VTS). pp. 1–6. IEEE (2014).

27. Segura, J.A., Champac, V.H., Rodríguez-Montañés, R., Figueras, J., Rubio, J.A.: Quiescent current analysis and experimentation of defective CMOS circuits. J. Electron. Test. 3, 337–348 (1992).
28. Dilillo, L., Girard, P., Pravossoudovitch, S., Virazel, A., Bastian, M.: Resistive-open defect injection in SRAM core-cell. In: Proceedings of the 42nd annual conference on Design automation - DAC '05. p. 857. ACM Press, New York, New York, USA (2005).
29. Vatajelu, E.I., Bosio, A., Dilillo, L., Girard, P., Todri, A., Virazel, A., Badereddine, N.: Analyzing resistive-open defects in SRAM core-cell under the effect of process variability. In: 2013 18TH IEEE EUROPEAN TEST SYMPOSIUM (ETS). pp. 1–6. IEEE (2013).
30. Fonseca, R.A., Dilillo, L., Bosio, A., Girard, P., Pravossoudovitch, S., Virazel, A., Badereddine, N.: Analysis of resistive-bridging defects in SRAM core-cells: A comparative study from 90nm down to 40nm technology nodes. In: 2010 15th IEEE European Test Symposium, ETS'10. pp. 132–137 (2010).
31. Fonseca, R.A., Dilillo, L., Bosio, A., Girard, P., Pravossoudovitch, S., Virazel, A., Badereddine, N.: Impact of Resistive-Bridging Defects in SRAM Core-Cell. In: 2010 Fifth IEEE International Symposium on Electronic Design, Test & Applications. pp. 265–269. IEEE (2010).
32. Copetti, T.S., Medeiros, G.C., Poehls, L.M.B., Balen, T.R.: Analyzing the Behavior of FinFET SRAMs with Resistive Defects. In: 2017 IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC). pp. 1–6. , Abu Dhabi (2017).
33. Intel: Intel's 14 nm Technology: Delivering Ultrafast, Energy-Sipping Products. (2017).
34. Samsung: Samsung Mass Produces 14-Nanometer Exynos Processor with Full Connectivity Integration. (2016).
35. Nanoscale Integration and Modeling (NIMO): Predictive Technology Model (PTM), http://ptm.asu.edu/.
36. Hisamoto, D., Kaga, T., Kawamoto, Y., Takeda, E.: A fully depleted lean-channel transistor (DELTA)-a novel vertical ultra thin SOI MOSFET. In: International Technical Digest on Electron Devices Meeting. pp. 833–836. IEEE (1989).
37. Bhattacharya, D., Jha, N.K.: FinFETs: From Devices to Architectures. Adv. Electron. 2014, 1–21 (2014).
38. Simsir, M.O., Bhoj, A., Jha, N.K.: Fault modeling for FinFET circuits. In: 2010 IEEE/ACM International Symposium on Nanoscale Architectures. pp. 41–46. IEEE (2010).
39. Karl, E., Wang, Y., Ng, Y.G., Guo, Z., Hamzaoglu, F., Meterelliyoz, M., Keane, J., Bhattacharya, U., Zhang, K., Mistry, K., Bohr, M.: A 4.6 GHz 162 Mb SRAM design in 22 nm tri-gate CMOS technology with integrated read and write assist circuitry. IEEE J. Solid-State Circuits. 48, 150–158 (2013).
40. Jan, C.H., Bhattacharya, U., Brain, R., Choi, S.J., Curello, G., Gupta, G., Hafez, W., Jang, M., Kang, M., Komeyli, K., Leo, T., Nidhi, N., Pan, L., Park, J., Phoa, K., Rahman, A., Staus, C., Tashiro, H., Tsai, C., Vandervoorn, P., Yang, L., Yeh, J.Y., Bai, P.: A 22nm SoC platform technology featuring 3-D tri-gate and high-k/metal gate, optimized for ultra low power, high performance and high density SoC applications. Tech. Dig. - Int. Electron Devices Meet. IEDM. 44–47 (2012).
41. Burnett, D., Parihar, S., Ramamurthy, H., Balasubramanian, S.: FinFET SRAM design challenges. In: 2014 IEEE International Conference on IC Design & Technology. pp. 1–4. IEEE (2014).
42. Liu, Y., Xu, Q.: On modeling faults in FinFET logic circuits. In: 2012 IEEE International Test Conference. pp. 1–9. IEEE (2012).