A 65 nm CMOS Synthesizable Digital Low-Dropout Regulator Based on Voltage-to-Time Conversion with 99.6% Current Efficiency at 10-mA Load

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Abstract. A synthesizable digital LDO implemented with standard-cell-based digital design flow is proposed. The difference between output and reference voltages is converted into delay difference using inverter chains as voltage-controlled delay lines, then compared in the time-domain. Since the time-domain difference is straightforwardly captured by a simple DFF-based phase detector, the proposed LDO does not need an analog voltage comparator, which requires careful manual design. All the components in the LDO can be described with Verilog codes based on their specifications, and placed-and-routed with a commercial EDA tool. This automated layout design relaxes the burden and time of implementation, and enhances process portability. The proposed LDO implemented in a 65 nm standard CMOS technology occupies 0.015 mm^2 area. With 10.4 MHz internal clock, the tracking response of the LDO to 200 mV switching in the reference voltage is ~4.5 μs and the transient response to 5 mA change in the load current is ~6.6 μs. At 10 mA load current, the quiescent current consumed by the LDO core is as low as 35.2 μA, which leads to 99.6 % current efficiency.

1 Introduction

Along with the exponential advancement of process technologies, performance of LSI circuits rapidly improves and many functional building blocks such as analog, logic, RF, memory block, etc. can be integrated on a chip, which have brought system-on-a-chip (SoC) era. Meanwhile, in order to reduce power consumption as indicated by the scaling law, power supply voltages have been lowered. In addition, it is desirable that a power supply of each functional block is independently tuned according to the changing operating condition so as to have the optimal power efficiency. The on-chip voltage regulation is essential for this purpose, because off-chip voltage regulators require large PCB area, which leads to increase in cost. For those reasons, efficient, tunable, fast-transient and on-chip power sources are in great demand for SoC, hence low-dropout (LDO) regulators are now widely used. As shown in Fig. 1(a), conventional LDOs have been designed with analog circuits and employed an error amplifier, a

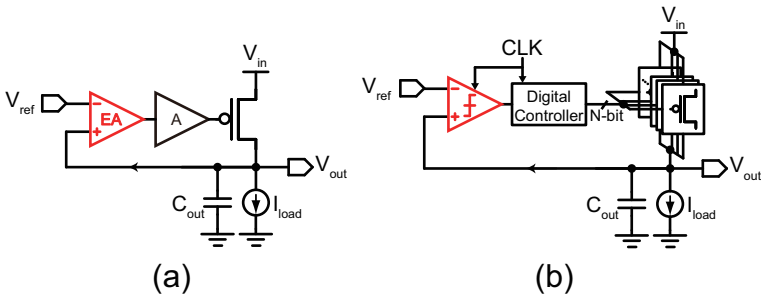

Fig. 1. LDO architectures. (a) Conventional analog LDO has a simple architecture, and includes an error amplifier, a driver amplifier and an analog pass transistor. (b) Digital LDO includes a comparator, a digital controller made of logic gates, and parallel pass transistors.

driver amplifier and an analog pass transistor to provide voltage regulation with negative feedback. When the supply voltage is high enough, they exhibit high current efficiency, fast transient response, high power supply rejection and small output ripple [1–4]. In addition, their area occupation could be smaller than other power management circuits such as switching regulators, because they do not require large inductors. However, they have difficulty in operating at low supply voltage, since amplifiers cannot sustain their dynamic range and high gain under such a situation. To solve this issue, the digital implementations of LDOs shown in Fig. 1(b) has been proposed [5–15]. A typical digital LDO has a digital controller made of logic gates that controls the number of turned-on PMOS switches at output stage, and employs an analog voltage comparator to detect the difference between reference and feedback voltages. Thus digital LDOs can eliminate amplifiers and operate under a low supply voltage. Moreover, since they are constucted mainly from digital logic gates, their performance can be easily improved by process downscaling and clock boosting.

A voltage comparator, however, often requires careful manual design so as to minimize the voltage offset between two inputs. Thus even digital LDOs also require sophisticated analog design flows, which is often time-consuming. A digital design flow, on the other hand, requires much less design effort, because its layout design is automated. Since circuit implementation in digital design flows is based on RTL source codes, the circuits that have the similar specification can be made easily even when the used process technologies are updated. Thus recently many analog circuits such as analog-to-digital converters (ADC) [16] or phase-locked loops (PLL) [17] are designed through digital automated flow, in order to take advantage of the relaxed design burden and process portability. Hence we have been motivated to implement LDOs, one of the indispensable blocks for SoCs, in digital design flows.

In order to relax the burden of manual analog designs, this paper proposes a synthesizable digital LDO, whose preliminary results have been presented in [18]. By utilizing voltage-to-time conversion, the proposed LDO has a suitable architecture for standard-cell-based automatic place and route (P&R).

2 Proposed Synthesizable LDO

2.1 Architecture

One of the design issues in constructing an LDO with standard cells is an implementation of a voltage comparison unit. Reference [16] reported that an analog voltage comparator can be implemented with 3-input NAND gates. Such comparators can be easily designed, but they suffer from the random systemtic offset owing to the randomness of the automatic P&R. Thus the single comparator made of NAND gates is not suitable for precise voltage comparison. The PLL-like LDO in [6] employs voltage-controlled ring oscillators in order to convert the voltage difference into the phase difference. However, this architecture is not preferable because a voltage-controlled ring oscillator has an integral characteristic that adds a pole to the system, which deteriorates the stability of the loop. Moreover, voltage-controlled ring oscillators might be a cause to increase the current consumption of the voltage comparison unit. Some digital LDOs utilize voltage-to-time converters (VTC) and time-to-digital converters (TDC) [7,8], so that they exclude analog voltage comparators. Although a TDC can be composed of digital logic cells, its layout implementation actually requires manual design because its linearity is very sensitive to the parasitic capacitance of its layout pattern. Hence we propose to use a simple bang-bang detector, in order to relax the complexity of the layout and eliminate the systematic offset even when the layout is automatically placed and routed.

Our proposed LDO shown in Fig. 2 employs voltage-controlled delay lines (VCDL), and the difference between the reference and the output voltages are converted into the time-domain. The proposed LDO consists of two inverter chains, a bang-bang phase detector, a digital controller, a PMOS switch array, and an output capacitor. Though for this prototype a dedicated ring oscillator is used as an internal clock source and a pulse generator, these clock and pulse signals can be replaced by a clock for other blocks on the SoC. The digital controller generates 128-bit-width thermometer code from 1-bit output from the bang-bang phase detector to control the switches. The PMOS switch array has parallelly-aligned 128 PMOS transistors, all of which have the same size. Each gate of the switch is connected to each bit of the thermometer code from the digital controller. The two inverter chains have the same structure, which has a series connection of 128 inverters. As shown in Fig. 3, the bang-bang phase detector is simply composed of a D-FF and a buffer. The buffer is connected to the clock input of the D-FF to compensate the setup time of the D-FF. As shown in Fig. 4, the internal clock and pulse generator is composed of inverters, D-FFs, and multiplexers for frequency tuning. The output capacitor is assembled off-chip. Once the switch PMOS transistor cell is added to a standard-cell library, all cells needed to compose the proposed LDO are included in the library and the LDO can be generated from Verilog gate-level netlists and synthesized with a P&R tool.

The layout of the PMOS switch has to follow the design rules for standard cells so that it can be placed and routed by the P&R tool. Fig. 5 shows an outline of the PMOS switch cell layout. It is designed just by removing the NMOS transistor from the inverter cell for ease of the additional cell layout. Thus, the size of the PMOS switch cell is equal to that of the inverter cell.

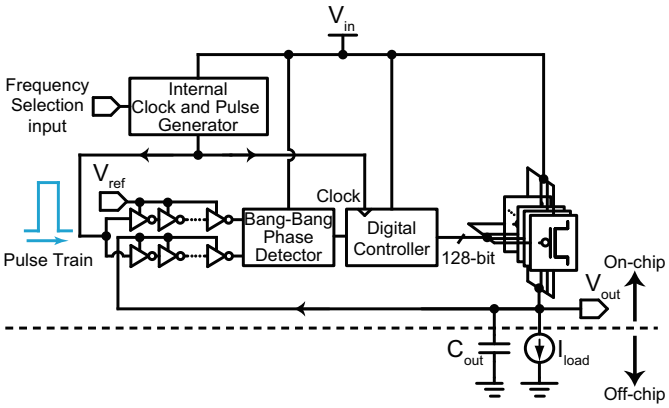

Fig. 2. Block diagram of the proposed LDO.

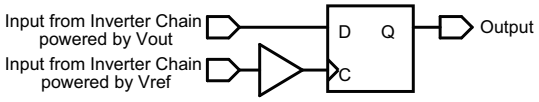

Fig. 3. Phase detector composed of standard cells.

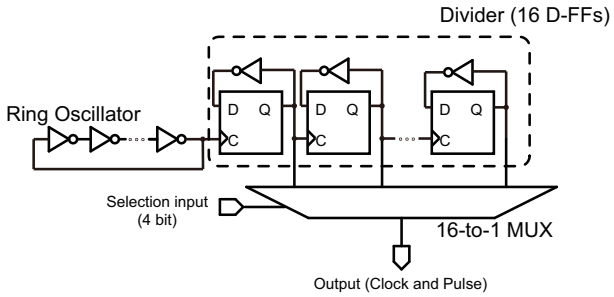

Fig. 4. Internal clock and pulse generator composed of a ring oscillator, a divider, and a multiplexer.

The operation of the proposed LDO is described as follows. As shown in Fig. 2, the two inverter chains are powered by V_{ref} and V_{out}, respectively. An identical pulse train from the internal pulse generator enters into them at the same time. The inverter chains work as VCDLs. In other words, the inverter chains convert the voltage difference between V_{ref} and V_{out} into the delay difference that is compared by the phase detector. Based on the phase detector output, the digital controller changes the number of turned-on PMOS switches.

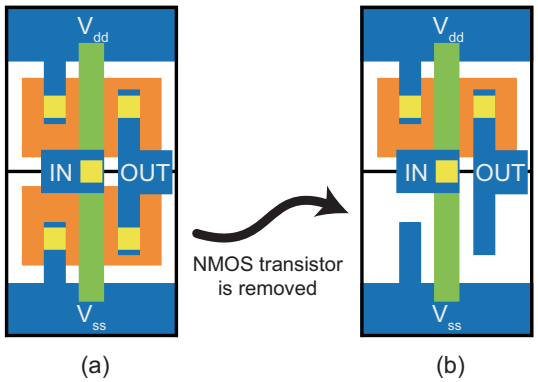

Fig. 5. (a) An inverter cell and (b) an additional PMOS transistor cell for the switch array.

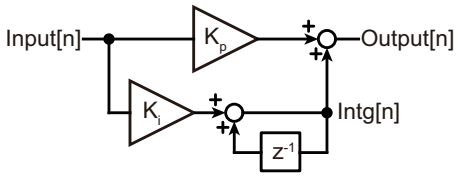

Fig. 6. Signal flow graph of the digital controller that includes proportional and integral paths.

Fig. 6 shows the signal flow graph of the digital controller. The operation of the digital controller is expressed by the following discrete-time difference equations.

$$\mathrm{Intg}[n] = \mathrm{Intg}[n-1] + K_i \times \mathrm{Input}[n] \tag{1}$$

$$\mathrm{Output}[n] = \mathrm{Intg}[n] + K_p \times \mathrm{Input}[n] \tag{2}$$

The digital controller includes proportional and integral paths. Output[n] is 7-bit binary. Then the binary output is decoded into thermometer code so that the number of turned-on PMOS switches can be controlled one by one. When V_{out} is higher than V_{ref}, the phase detector output becomes HIGH and the digital controller decreases the number of turned-on switches. On the contrary, when V_{out} is lower than V_{ref}, the phase detector output becomes LOW and the digital controller increases the number of turned-on switches. In this way V_{out} approaches to V_{ref}. As the divider and the multiplexer is attached to the internal clock and pulse generator, in this prototype the clock frequency can be easily tuned by the multiplexer for test purpose.

The components other than the inverter chains are powered by V_{in}. The HIGH-level voltage of the pulse trains which travel through the inverter chains are equal to their power source voltage, V_{ref} or V_{out}. Therefore, if V_{ref} is lower than the logic threshold voltage of the phase detector powered by V_{in}, the phase detector cannot be driven by the pulse from the inverter chain powered by V_{ref}. Thus, the lower limit of V_{ref} is determined by the logic threshold voltage of the standard cells powered by V_{in}.

2.2 Transfer Function of the Control Loop

Fig. 7 shows the signal flow graph of the proposed LDO. The comparison unit composed of inverter chains and a D-FF generates an error sample. Since the comparison is done based on the pulse train which is the same signal as the clock, one clock delay occurs here at every sample. As previously described, the digital controller has proportional and integral paths. In order to investigate the loop stability in continuous-time domain, the approximation below is applied:

$$z \approx 1 + sT_s, \tag{3}$$

where T_s represents the sampling period. The transfer function of the digital controller is thus approximated as follows:

$$H_{ctrl} = K_p + \frac{1}{1 - z^{-1}} K_i \tag{4}$$

$$\approx K_p + \frac{1 + sT_s}{sT_s} K_i. \tag{5}$$

The output stage is composed of the switch array, the output capacitor, and the effective resistance. I_{pmos} is the current through a single PMOS switch. According to [9], the effective resistance R_l can be approximated as V_{out}/I_{load}. Using (3) and (5), the continuous-time open-loop transfer function $G(s)$ is given by

$$G(s) = \left(\frac{K_p}{1 + sT_S} + \frac{K_i}{sT_s} \right) \cdot \frac{I_{pmos}}{R_l^{-1} + sC_{out}}. \tag{6}$$

When I_{load} is small, R_l becomes big so that $R_l^{-1} \ll sC_{out}$. Then, $G(s)$ approximates

$$G(s) \approx \left(\frac{K_p}{1 + sT_S} + \frac{K_i}{sT_s} \right) \cdot \frac{I_{pmos}}{sC_{out}}. \tag{7}$$

If $K_p = 0$, the poles of the closed-loop transfer function are close to the imaginary axis, and thus the system tends to be unstable. To avoid oscillation, we add the proportional gain K_p to the digital controller. Fig. 8 shows the bode plots of the open loop transfer function with small I_{load} of 100 µA for $K_P = 0$ and $K_p = 1$, respectively. When $K_p = 0$, the phase margin is 17°, whereas it is 27° when $K_p = 1$, which suppresses the abrupt phase change around 1 MHz.

2.3 Design Procedure of the Proposed LDO

This section explains the design procedure of the proposed LDO. Fig. 9 shows the design flow diagram. The explanation follows the step numbers shown in Fig. 9. 0) The PMOS switch cell is designed in advance and added to the standard-cell library. 1) The specification of the circuit, such as maximum load current or reference voltage, is set. Based on this specification, the number of the PMOS switches in the switch array and the output bit width of the digital controller are determined. 2) The RTL Verilog code of the digital controller is prepared, then logically synthesized to have

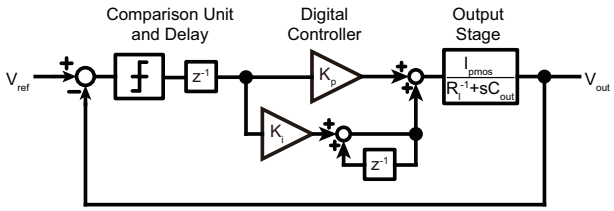

Fig. 7. Signal flow graph of the proposed LDO.

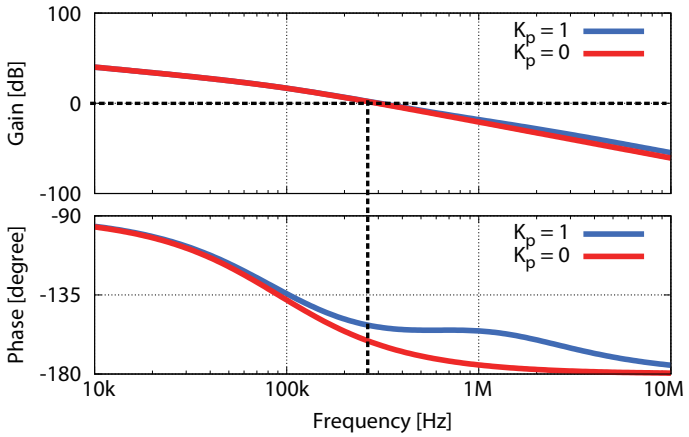

Fig. 8. Bode plots of the open loop system with the small I_{load} of 100 µA for $K_P = 0$ and $K_p = 1$.

the gate-level Verilog netlist. 3) The gate-level Verilog netlists of other components, such as the inverter chain, the phase detector, the switch array, and the internal clock and pulse generator are generated by a dedicated script. Examples of the gate-level Verilog description is shown in Fig. 10. Since each building block has simple standard-cell-based structure, the gate-level netlist generation is simply implemented. For example, the switch array is constructed only by the parallel PMOS switch cells, and thus its gate-level netlist is generated easily by the script according to the specification. 4) The layout of each building block is individually placed and routed by a P&R tool. This is because they have different power supplies; the two inverter chains are powered by V_{out} or V_{ref} respectively, and the other blocks are powered by V_{in}. We use the same layout for both of the two inverter chains, so that there is little systematic offset in the voltage comparison unit. 5) All the layouts are connected together. It takes few hours to generate the whole layout of the proposed LDO from scratch, which is much less time than that in the case for the conventional LDO design with analog flows.

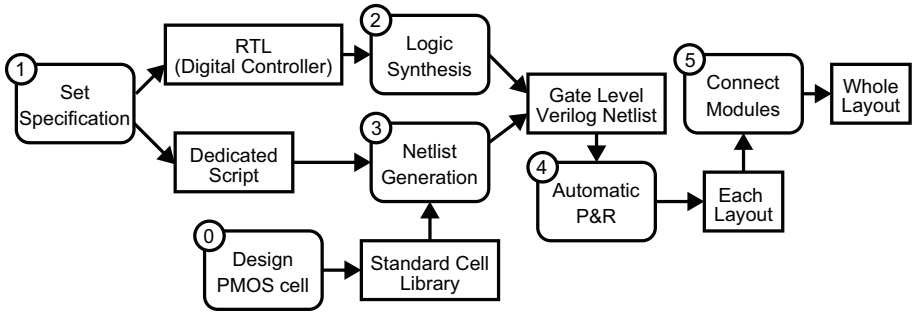

Fig. 9. Design flow of the proposed circuit.

(a)
```
module inverterChain(IN, OUT);
    input IN;
    output OUT;
    wire node0, node1, ..., node(K-1);

    inv U0 (.A(IN), .Y(node0));
    inv U1 (.A(node0), .Y(node1));
    ...
    inv UK (.A(node(K-1)), .Y(OUT));
endmodule
```

(b)
```
module phaseDetector(INP, INN, OUT);
    input INP, INN;
    output OUT;
    wire node0;

    buf U0 (.A(INN), .Y(node0));
    dff U1 (.D(INP), .C(node0), .Q(OUT));
endmodule
```

(c)
```
module switchArray(IN, OUT);
    input [N-1:0] IN;
    output OUT;

    pmos U0 (.A(IN[0]), .Y(OUT));
    pmos U1 (.A(IN[1]), .Y(OUT));
    ...
    pmos U(N-1) (.A(IN[N-1]), .Y(OUT));
endmodule
```

(d)
```
module clockAndPulseGenerator(SELECT, OUT);
    input [1:0] SELECT;
    output OUT;
    wire node0, node1, node2,
         q0, q1, q2, q3,
         xq0, xq1, xq2, xq3;

    // ring oscillator
    inv U0 (.A(node2), .Y(node0));
    inv U1 (.A(node0), .Y(node1));
    inv U2 (.A(node1), .Y(node2));
    // divider
    dff U3 (.D(xq0), .C(node2), .Q(q0));
    inv U4 (.A(q0), .Y(xq0));
    dff U5 (.D(xq1), .C(q0), .Q(q1));
    inv U6 (.A(q1), .Y(xq1));
    dff U7 (.D(xq2), .C(q1), .Q(q2));
    inv U8 (.A(q2), .Y(xq2));
    dff U9 (.D(xq3), .C(q2), .Q(q3));
    inv U10 (.A(q3), .Y(xq3));
    // multiplexer
    mul U11 (.A(q0), .B(q1), .C(q2), .D(q3),
             .S0(SELECT[0]), .S1(SELECT[1]),
             .Y(OUT));
endmodule
```

Fig. 10. Examples of the gate-level Verilog description: (a) inverter chain, (b) phase detector, (c) switch array, and (d) internal clock and pulse generator.

3 Prototype Implementation and Measurement Results

Based on the architecture described in the previous section, the prototype of the proposed LDO is fabricated in a 65 nm standard CMOS technology. Fig. 11 shows the chip photo. The active area of the proposed LDO is 0.015 μm^2.

Fig. 12 shows the measured tracking response of V_{out} with 10.4 MHz clock when V_{ref}, which is externally supplied in this measurement, switches between 600 mV and 800 mV. Here, I_{load} and C_{out} is 10 mA and 220 pF, respectively. When V_{ref} changes from 600 mV to 800 mV, the settling time is 4.5 µs, whereas it is 4.4 µs when V_{ref} changes from 800 mV to 600 mV. Fig. 13 shows the measured transient response of V_{out} with 10.4 MHz clock when I_{load} changes between 5 mA and 10 mA. V_{ref} of 800 mV and C_{out} of 220 pF are used in this experiment. When I_{load} changes from 5 mA to 10 mA, the

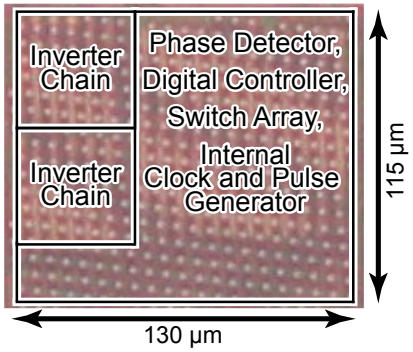

Fig. 11. Chip photo of the proposed LDO that occupies 115 µm × 130 µm in 65 nm standard CMOS technology.

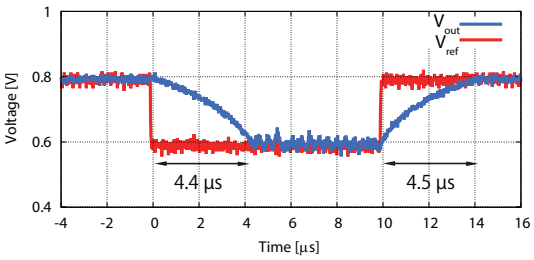

Fig. 12. Measured tracking response of V_{out} when V_{ref} switches between 600 mV and 800 mV with 10.4 MHz-clock, I_{load} of 10 mA and C_{out} of 220 pF.

settling time is 6.6 µs and the undershoot is 303 mV. When I_{load} changes from 10 mA to 5 mA, the settling time is 6.0 µs and the overshoot is 126 mV. Since the operation region of PMOS temporarily enters into saturation region when the undershoot occurs while it does not for the case of overshoot, the waveforms of V_{out} transient become different in these two cases.

The overall current consumption with 10.4 MHz clock and I_{load} of 10 mA is 282 µA including the current consumed at the internal clock and pulse generator, which is not essential in the actual use because it can be substituted by an internal clock for other functional blocks on the SoC. Based on the circuit simulation result, the LDO core consumes 12.5 % of the total current as shown in Fig. 14. Thus, the quiescent current of the LDO core is assumed to be 35.2 µA, which leads to 99.6 % current efficiency.

In the proposed architecture, V_{ref} is used as a power source of a VCDL. Hence, V_{ref} is required to supply current to drive the VCDL for voltage comparison. Fig. 15 shows the current consumption from V_{ref} versus the frequency of the pulse train, which is equal to CLK, with V_{ref} of 800 mV and I_{load} of 10 mA. The pulse is sent from the internal oscillator, and its frequency is tuned by the multiplexer. Typically, when the

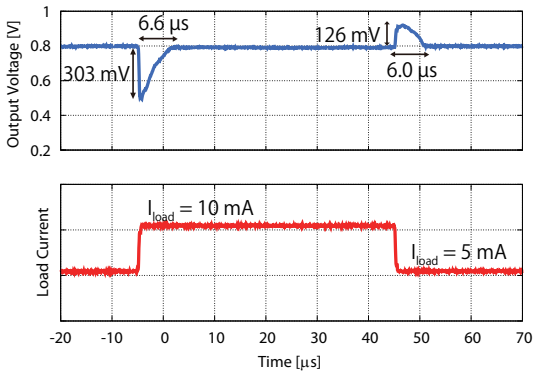

Fig. 13. Measured transient response of V_{out} when I_{load} changes between 5 mA and 10 mA with 10.4 MHz-clock, V_{ref} of 800 mV and C_{out} of 220 pF.

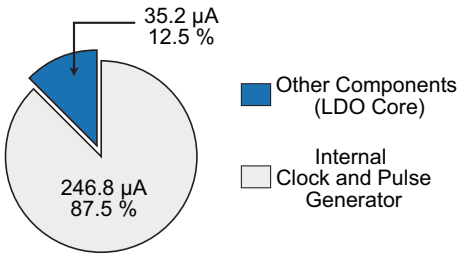

Fig. 14. Breakdown of the current consumption with I_{load} of 10 mA. Ratio of the current is calculated with circuit simulation.

pulse frequency is 10.4 MHz, the current consumption from V_{ref} is 10.6 µA. According to Fig. 15, the current consumption of V_{ref} is proportional to the pulse frequency. When the pulse frequency is set high in order to have the fast transient response, V_{ref} is required to supply more current.

Table 1 shows performance comparison to prior digital LDOs. This work realizes a competitive current efficiency and $\mathrm{FOM_T}$ with synthesizable architecture, while others cannot be fully synthesizable and need manual designs. Owing to the automated design flow of this work, if needed the maximum load current $I_{load,max}$ can be easily increased by adding more PMOS switches, at the expense of the increase in the area and the quiescent current.

4 Conclusion

This paper proposes a synthesizable digital LDO that is designed by a P&R tool. In the proposed LDO, by using inverter chains as VCDLs, the difference between the output and the reference voltages is converted into the delay difference that can be compared

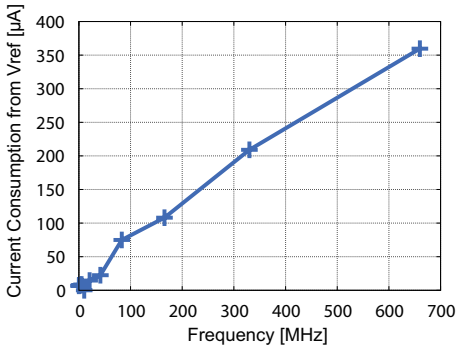

Fig. 15. Current consumption from V_{ref} versus the frequency of the pulse train.

Table 1. Comparison to prior arts of Performance

	This work	[5] CICC 2010	[6] JSSC 2014	[10] JSSC 2017	[11] JSSC 2018	[12] SSC-L 2018	[13] TPE 2018	[14] SSC-L 2018
Process	65 nm	65 nm	32 nm	65 nm	65 nm	65 nm	65 nm	28 nm
Active area [mm^2]	0.015	0.042	0.008	0.029	0.0023	0.012	0.014	0.019
V_{in} [V]	1.0	0.5	0.7-1.0	0.5-1.0	0.5-1.0	0.5-1.0	0.7-1.2	0.6-0.65
V_{out} [V]	0.8	0.45	0.5-0.9	0.45-0.95	0.3-0.45	0.35-0.95	0.6-1.1	0.55-0.6
$I_{load,max}$ [mA]	10	0.2	5	3.5	2	2.8	25	25
C_{out} [pF]	220	100000	100	400	400	100	1000	150
Quiescent I_q [μA]	35.2	2.7	92	12.5	14	45.2	6	28
Current efficiency [%]	99.6	98.7	98.2	96.3	99.8	98.4	99.97	99.96
Transient ΔV_{out} @ load step ΔI_{load}	300 mV @ 5 mA	40 mV @ 0.2 mA	150 mV @ 0.8 mA	40 mV @ 0.4 mA	40 mV @ 1.06 mA	46 mV @ 1.76 mA	200 mV @ 23.5 mA	56 mV @ 20 mA
FOM_T [ps]*	93	270000	1150	1250	199	67.1	2.17	0.59

*$FOM_T = (C_{out} \times \Delta V_{out} \times I_q)/\Delta I_{load}^2$ [1]

by a phase detector. The voltage control loop is all composed of standard cells and synthesizable, which drastically relaxes the design burden. The prototype is fabricated in a 65 nm standard CMOS technology with 0.015 mm^2 area occupation. According to the measurement results of the prototype, with 10.4 MHz clock and C_{out} of 220 pF the tracking response time when V_{ref} switches between 600 mV and 800 mV is ~4.5 μs with I_{load} of 10 mA, and the transient response time when I_{load} changes between 5 mA and 10 mA is ~6.6 μs with V_{ref} of 800 mV. The quiescent current consumed by the LDO core is as low as 35.2 μA at 10 mA load current, which leads to 99.6 % current efficiency. In our prototype, V_{ref} needs to supply 10.6 μA current when the pulse frequency is 10.4 MHz.

In this paper, we used a PMOS switch cell made from an inverter cell. However, this customized PMOS switch cell can be substituted by a tri-state inverter cell [15] or a tri-state buffer cell. If the inputs of these cells are tied to LOW (in the case of tri-state inverters) or HIGH (in the case of tri-state buffers), the output PMOS transistors can be controlled by the tri-state control inputs. Thus, if these cells are included in the standard

cell library, a fully standard-cell based synthesizble LDO can be realized and the design burden would be more relaxed.

5 Acknowledgment

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