Adaptive Transceiver for Wireless NoC to Enhance Multicast/Unicast Communication Scenarios

Joel Ortiz Sosa, Olivier Sentieys, Christian Roland

2019 IEEE Computer Society Annual Symposium on VLSI (ISVLSI)

Adaptive Transceiver for Wireless NoC to Enhance Multicast/Unicast Communication Scenarios

Joel Ortiz Sosa
Univ Rennes, Inria
Lannion, France
joel.ortiz-sosa@inria.fr

Olivier Sentieys
Univ Rennes, Inria
Rennes, France
olivier.sentieys@inria.fr

Christian Roland
UBS - Lab-STICC
Lorient, France
christian.roland@univ-ubs.fr

***Abstract*—Wireless Network-on-Chip (WiNoC) is a viable solution to overcome critical bottlenecks in on-chip communication backbone. However, standard WiNoC approaches are vulnerable to multi-path interference introduced by on-chip physical structures. To overcome such parasitic phenomenon, this paper presents an adaptive digital transceiver, which enhances communication reliability under different wireless channel configurations. Based on a semi-realistic wireless channel model, we investigate the impact of using some channel correction techniques. Experimental results show that our approach significantly improves Bit Error Rate (BER) under different wireless channel configurations. Moreover, our adaptive transceiver allows for wireless communication links to be established in conditions where this would not be possible for standard transceiver architectures. The proposed architecture, designed using a 28-nm FDSOI technology, consumes only 3.27 mW for a data rate of 10 Gbit/s and has a very small area footprint.**

***Index Terms*—Wireless Network-on-Chip, Communication Reliability, Adaptive Digital Transceiver Architecture**

I. Introduction

The number of cores integrated into current system-on-chip (SoC) architectures is still expected to grow significantly in the future. The Network-on-Chip (NoC) paradigm has been proposed as a solution that can scale with the number of cores. However, with technology scaling and performance limitation of metal interconnects in advanced technologies, the number of cores interconnected by a NoC is reaching a limit. Furthermore, critical bottlenecks are created due to multiple unicast and multicast/broadcast network traffic schemes, thus highly increasing latency and power consumption. To deal with these issues, new interconnect technologies have emerged, *e.g.*, 3D-NoC [1], RF Interconnects (RF-I) based on waveguides [2], Optical NoC [3] and Wireless NoC [4].

Wireless Network-on-Chip (WiNoC) peculiarly fulfills system feasibility and flexibility to overcome limitations of standard wired communications. However, the reliability of wireless links is not enough explored and remains an important and unsolved issue. For instance, current WiNoC works rely on a simplistic wireless propagation channel, which only considers path loss through free space and Additive White Gaussian Noise (AWGN). Nevertheless, physical structures and silicon properties can easily introduce parasitic phenomena (*e.g.*, multi-path propagation), especially when communication data rate is aiming at several tens of gigabits per second. Furthermore, since cache coherence is a protocol commonly supported by NoCs, various communication scenarios are important to be considered during the wireless network design, such as many-to-one, all-to-one and multiple-unicast. As a consequence, multiple channel access is also a meaningful issue to be solved by WiNoC systems to take full advantage of wireless links.

In this paper, we propose a reconfigurable digital transceiver architecture with efficient support of unicast/broadcast, many-to-one, all-to-one, and multiple unicast communication patterns, adopting some configurable channel compensation techniques. We show that it is required to adapt the transceiver configurations according to these different communication patterns, in order to improve WiNoC performance, especially when facing a semi-realistic wireless channel. Furthermore, the design adopted provides low complexity, sustains low bit-error-rate, minimal data transfer latency and reasonable power requirements. Indeed, each configuration is intended to be used according to network traffic requirements.

The rest of the paper is organized as follows. Section II highlights the main limitations in the state-of-the-art of current WiNoC architectures. Section III shows the general WiNoC architecture used in this work. Section IV presents the adopted semi-realistic channel model. In Section V, we study the channel cancellation techniques to overcome multi-path propagation, as well as the adopted technique to provide multiple channel accesses. In Section VI, we propose a new transceiver architecture. Finally, in Section VII, we show some performance and synthesis results of the proposed architecture before to conclude in Section VIII.

II. Related Work

Conventional Network-on-Chip architectures forward data packets through several or many routers/switches. The multi-hop nature of this type of topology contributes significantly to power consumption and latency overheads due to data transfers. WiNoCs were proposed as a promising solution due to their one-hop nature of data transfer, seamless integration with current chip fabrication process and scalablility of the network with ever-larger number of cores. However, since current wireless transceiver overheads are not negligible, the architecture adopted for WiNoCs is mostly hybrid and typically combines wireless and electrical interconnects.

The modulation scheme adopted by most WiNoC solutions is On-Off Keying (OOK). Providing low complexity design

978-1-7281-3391-1/19/$31.00 ©2019 IEEE
DOI 10.1109/ISVLSI.2019.00111

implementation compared to other modulation schemes. The transceivers designed with this modulation are based on coherent [5] or non-coherent [6] detection with hard decision avoiding the use of analog-to-digital converter (ADC). Indeed, other modulation schemes (BPSK, QPSK, 16-QAM, *etc.*) can provide better spectral efficiency and higher resilience to channel interference, but at the cost of consuming much more power and area than OOK.

Most contributions in the WiNoC research field are oriented to demonstrate that WiNoCs can overcome limitations of conventional NoC architectures for core-to-core [7], and core-to-memory communications, *e.g.*, in the case of cache coherency [8]. Contributions have also investigated different network topologies to take advantage of long distance links [7]. Additionally, there is a substantial body of work analyzing the impact of allowing multiple parallel channel accesses to improve bandwidth, average packet energy and communication latency. These approaches mainly divide the channel by creating multiple isolated spaces (SDM) [9], by frequency (FDM) [10], using orthogonal frequencies (OFDM) [2], [11], and adopting channelization codes (CDM) [12]. However, each parallel channel access method comes with some challenges to be implemented in WiNoC, such as early network saturation, several band-pass filters, frequency synthesizers, (inverse) fast Fourier transform blocks and ADCs.

Current WiNoC architectures are evaluated using very simple wireless channel model, *i.e.*, considering AWGN as the only impairment in the communication. However, the AWGN model is not representative of actual intra-chip wireless channels. In particular, it does not consider the frequency selectivity and time behavior of WiNoC for isotropic antennas, such as multi-path propagation and bandwidth limitation. Few prior works have introduced some interesting channel features that could have been considered for WiNoC simulations. For instance, a two-ray signal propagation and molecular absorption attenuation (MAA) were introduced in [13] and [14], respectively. Further, a proof-of-concept study was performed in [15] using isotropic integrated dipole antennas in ka band (26-40 GHz). This study proves the multi-path nature of WiNoC channel, as well as the problems related to silicon properties.

III. WiNoC Architecture

For NoC architectures, hybrid interconnects are more suitable designs to improve throughput, power consumption, and scalability than using only one interconnect type. This premise is demonstrated in WiNoC state-of-the-art where several approaches combine wired/wireless and optical/wireless [16] solutions. Combining wireless links with another interconnect solution allows for the number of embedded cores to be easily scaled and latency and power to be improved. This is due to the natural support of broadcast/multicast communication traffic in wireless links, which is especially difficult with a large number of cores (*e.g.*, 256 – 1024).

To manage the wireless channel, WiNoC solutions require a wireless interface (WI), typically connected to a conventional NoC router. This WI is divided into analog and digital parts. Current analog part typically comprises an OOK transceiver supporting 16 Gb/s data rate. The digital part includes a serializer/deserializer (SER/DESER) module and a wireless network access controller. Nevertheless, this basic WI only supports unicast or broadcast communications in a given time slot.

As power overhead limits the number of wireless links, creation of clusters (subnetworks of processing elements) is necessary during the topology design. Each cluster typically incorporates a single WI connected to one or several router/switches of the electrical NoC. However, multiple switches connected around the WI improves efficiency of the access to the wireless point from different cluster areas. The general WiNoC architecture considered in this work is depicted in Fig. 1. The wired interconnect network connects all the cores using a mesh topology. N clusters of M cores are distributed homogeneously on the chip with one WI connected to four routers. This configuration can easily scale with the number of cores embedded on the chip. Moreover, this kind of WiNoC architecture was already experimentally analyzed in [17] using a wired 16×16 mesh topology. The authors show that a wireless link utilization of 48% for real traffic scenarios leads to significant latency and energy improvements compared to an electrical-only NoC.

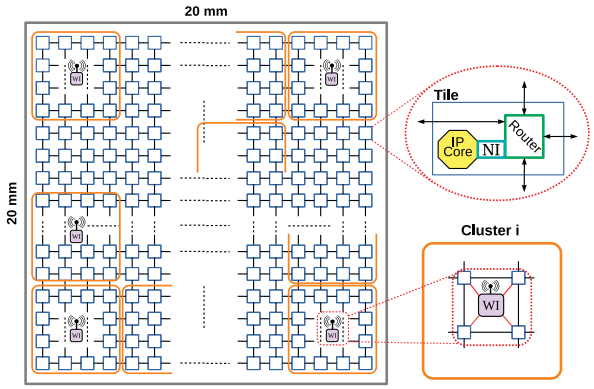

Fig. 1. Wireless interface distribution among a clustered WiNoC hybrid topology with N clusters of M cores.

IV. Channel Modeling

The WiNoC channel must be modeled considering the parasitic phenomena introduced by the physical structure and electrical properties of all the components inside the chip and by the chip package [14]. Therefore, the design of an accurate channel model for WiNoC applications is important but it is also a complex task. However, contrary to standard wireless communications, in WiNoC, the propagation medium can be characterized according to the chip fabrication process and considered as stationary.

Wave propagation properties over intra-chip wireless channels have been analyzed in [18], creating different ray paths through the silicon wafer. Demonstration of three wave propagation types (space, surface and guided wave) are analysed in [19] using different antenna types and surrounding elements

between the transmission and reception antenna. Besides, their analysis proves that the dominant path is propagated through the surface rather than the space.

The results presented in this paper are based on a semi-realistic channel model for intra-chip wave propagation derived from [14], [18], [19]. The channel impulse response (CIR) representation considers two main propagation paths: direct and reflected path. The direct and reflected path are separated in time by one symbol duration.The reflected path is generated by the edges of the chip. The amount of energy preserved by the reflected path after to be rebounded by the chip-edge structures, mainly depends of the physical structures and substrate losses. A rough approximation of this preserved energy was performed in [20], defining this energy as a ratio (α) between the amplitudes of the reflected and the direct path. In the rest of the paper, this ratio is considered as $\alpha = 60\%$ which, according to [20], corresponds to the worst condition of a channel without any mechanism to avoid chip-edge reflections.

V. Channel Compensation Techniques

As discussed in Section IV, intra-chip wireless propagation channel is affected by multi-path interference. Nevertheless, to the best of our knowledge, current WiNoC transceiver solutions do not incorporate any channel compensation mechanism considering different communication traffics. In [20], the author introduce a WI with different multi-path cancellation techniques which only supports many-to-one wireless communication patterns. In this paper, we propose a reconfigurable digital transceiver that is able to compensate for channel interference considering unicast/broadcast and multicast requirements. As compensation efficiency closely depends on the channel cancellation technique adopted, this solution employs a channel compensation technique according to the channel access configuration. This work complementary relies on a technique oriented to unicast/broadcast communication and a second one adapted to multiple channel accesses in parallel.

A. Decision Feedback Equalizer

The decision feedback equalizer (DFE) is an effective technique for detection of signal affected by noise and inter-symbol interference (ISI). As shown in Figure 2(a), the general structure of a DFE consists of a feedforward filter (FFF), a feedback filter (FBF) and a symbol detector [21]. Computation of FFF and FBF by methods operating entirely in the time domain has been widely studied in standard wireless communication literature [22]. This time domain analysis is performed to model both filters using the finite impulse response (FIR) transverse form. In this work, the DFE technique is used only for single channel access, since its performance is affected by decision errors and that any erroneous decision is propagated in the system, thus affecting the upcoming signal corrections.

As mentioned in Section IV, the WiNoC channel is time-invariant, causal and stable. Therefore, the DFE structure could be simplified without the FFF block and the form shown in

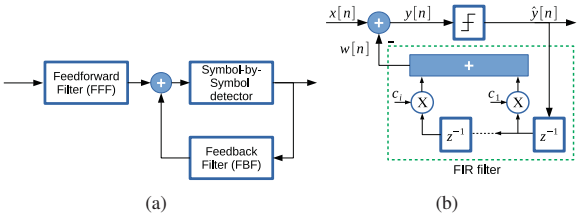

Fig. 2. (a) General DFE structure, (b) Adopted DFE.

Fig. 2(b) is adopted. Consequently, the correction signal $w[n]$ is subtracted from the sampled received signal $x[n]$. Then the corrected signal $y[n] = x[n] - w[n]$ is passed to a decision block whose output signal $\hat{y}[n]$ is given by

$$\hat{y}[n] = \begin{cases} 1 & y[n] \geq V_{th} \\ 0 & y[n] < V_{th} \end{cases}$$

where V_{th} is the threshold defined by the transmission system. The signal $\hat{y}[n]$ is the input signal of an FIR filter of length M_h with coefficients c_i, which generates the correction signal $w[n]$. The filter coefficients c_i are equal to the coefficients of the channel impulse response and M_h is also the length of the CIR. As an example, following the channel model discussed in Section IV, the filter is specified by $M_h = 2$, $c_0 = 0$, $c_1 = \alpha$, and $c_i = 0$, $\forall\, i \geq 2$.

B. Time Diversity Scheme

The Time Diversity Scheme (TDS) is based on Direct-Sequence Spread Spectrum (DSSS) modulation technique, which allows to take advantage of the multiple copies of the same signal created by the propagation channel. The effectiveness of this technique lies in the fact that each copy differs in time by one symbol (chip) duration. TDS is recognized as an efficient technique to compensate for channel interference in WiNoC communications [20]. However, unlike the architecture proposed in [20] assigning a dedicated code for each cluster, in this work, the codes are assigned dynamically, allowing us to easily manage the different multicast configurations.

The receiver architecture correlates the input data signal $x[n]$ with L code sequences delayed by $i = 0 \ldots L-1$ chip periods. The L correlator outputs are combined using a diversity combining rule with their respective weighting coefficients (G_i).

VI. Proposed Wireless Interface Architecture

Digital part of conventional WI is significantly modified to comply with the proposed adaptive techniques. Fig. 3 depicts the architecture of the proposed adaptive transceiver. An ADC is required to implement channel correction mechanisms and support multiple channel access. This ADC is constrained to have a low impact on area and power consumption. Therefore, the bit resolution and sampling frequency should be as low as possible, while keeping system integrity. Consequently, the ADC block adopted in this work is a 10 Giga-samples-per-second time-interleaved successive approximation register

(SAR) [23]. Providing eight 4-bit words in parallel at 1.25 GHz corresponding to eight consecutive samples.

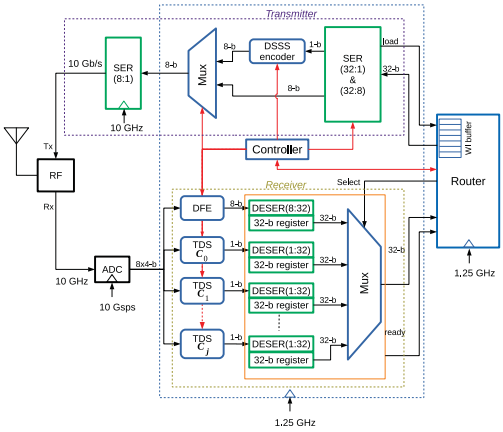

Fig. 3. Enhanced digital-domain transceiver architecture.

A. Adaptive Wireless Access

To take advantage of communication patterns and traffic variations, the wireless access is adaptive. In our case, adaptivity means that according to the communication scenarios (unicast, broadcast/multicast), the channel can be reserved by one or multiple WIs. In addition, each wireless node uses a half-duplex operation to avoid signal cancellation, self-interference, and to simplify the OOK transceiver design. The WIs are configured in transmission or reception mode according to system communication requirements. Fig. 4 depicts the different communication patterns that could be supported by the proposed adaptive wireless interface design. In this example, the hybrid topology has $N = 4$ clusters distributed on the chip, each one with one WI placed in the center of cluster. Increasing the number of cluster beyond $N = 4$ follows the same principle for the communication patterns.

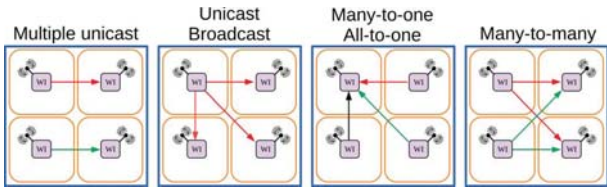

Fig. 4. Wireless communication patterns for a clustered WiNoC hybrid topology with $N = 4$ clusters.

Parallel Mode: The parallel mode corresponds to many-to-one, all-to-one, and multiple unicast communications, where several WIs require to use the wireless channel at the same time. In this case, a synchronous DSSS technique based on channelization codes is configured in each WI to allow for parallel communications. The maximum number of parallel communication is defined as $N-1$ clusters (all-to-one mode), with at least one cluster as a receiver. Once the number of source and destination clusters are defined, the available codes are selected randomly by each WI. These codes are released when all data are transmitted to the destination nodes.

Unicast/Broadcast Mode: In the second mode, unicast or broadcast communication is used. Therefore, one transmitter and one receiver (unicast) or multiple receivers (broadcast) are configured in the wireless network. As the channel does not need to be shared with other transmitters, no channelization code is necessary to forward information to the destination nodes. In this mode, the DFE compensation technique is used to enhance communication link reliability.

B. Digital Transmitter Architecture

As depicted in the upper part of Fig. 3, the transmitter is composed of three blocks: SER(32:1/8), DSSS encoder, and SER(8:1). A serializer SER(n:m) is a shift register having an input on n bits issued at a clock f_i which is serialized on an m-bit output at a clock $f_o = n.f_i/m$. The SER(32:1/8) has two outputs on 1 bit and 8 bits, which are activated according to system requirements. In case of unicast/broadcast communication, the SER(32:1/8) 8-bit output is multiplexed into the SER (8:1) block. Otherwise, when channel multiple access is required, the SER (32:1/8) 1-bit output and DSSS encoder blocks are activated by the controller.

The DSSS encoder is very simple, since composed of a register initialized by the considered 8-bit channelization code (C_j) or its complement, according to the input data being equal to 1 or 0, respectively. This encoder relies on the code C_j selected by the controller during the configuration phase. On the router/switch side, the output ports connected with the SER(32:1/8) block have an increased RF buffer depth of 8 flits (1 flit = 32 bits) to avoid excessive latency while waiting the channel to be released. As explained in [24], buffer depth beyond this limit does not produce any further performance, but leads to overhead in power and area.

C. Digital Receiver Architecture

As shown in the lower part of Fig. 3, the receiver is composed of blocks: DFE channel compensation, DESER(8:32), and one DESER(1:32) and TDS per code C_j. Each DESER is associated with a 32-bit register to store the flit before to be read by the router. All channel compensation blocks (DFE, TDS C_j) receive eight 4-bit words in parallel from the ADC. Furthermore, these blocks are only activated during the network configuration phase according to communication requirements. For the unicast/broadcast mode, the DFE and associated DESER(8:32) blocks are activated for channel compensation. For the parallel channel access mode, the TDS blocks are configured by the controller with allocated C_j. A TDS block consists of several correlators to act against multi-path interference existing in the CIR. Each TDS block is associated with a particular 8-bit channelization code C_j to allow for parallel communications. The data received from these blocks is deserialized in the respective DESER blocks (complexity similar to the SER) and saved into the 32-bit registers. Then, a signal is immediately sent to the router/switch indicating the register state.

VII. Hardware Implementation and Performance Evaluation

An end-to-end wireless communication system has been implemented for performance simulation and hardware synthesis. The effectiveness of this architecture is estimated under unicast/multicast conditions in presence of multi-path interference, as described in Section IV. The system under study is simulated using MATLAB assuming perfect synchronization to estimate the bit error rate (BER) performance. Then, the digital transceiver architecture is modeled in C/C++ for High-Level Synthesis (HLS). The design is synthesized from C to RTL by Catapult HLS (V10.8) and to the gate level by Synopsys Design Compiler (V2015.06-SP5). A 28-nm FDSOI technology library is used during hardware synthesis as a target with a supply voltage of 1 Volt. Finally, the full transceiver design was validated by simulation from the C/C++ model down to the gate level using ModelSim and SCVerify.

A. Bit Error Rate Evaluation

The end-to-end system modeled in MATLAB considers a half-duplex communication and consists of four wireless interfaces (*i.e.*, $N = 4$ clusters) configured for single or parallel communication. The channelization codes used during parallel channel access are orthogonal Hadamard codes on 8 bits, supporting up to 7 parallel channels. The channel model employed in the simulations is a two-ray time-invariant frequency-selective channel with AWGN. The modulation scheme simulated is coherent OOK. The simulated model considers the quantization noise added in the demodulation process by a 4-bit ADC at the receiver side. Finally, the average BER is estimated by Monte-Carlo simulation with a confidence interval of 95%. Simulation results are reported in Fig. 5 for single and parallel channel configurations. Their effectiveness is contrasted with the single channel simulated BER of OOK with multi-path using $\alpha = 0.6$ (60%), and without multi-path channel (OOK Theory in Fig. 5). As reported in [20], OOK without channel compensation is practically unsuitable for communications facing multi-path interference.

Firstly, the DFE and TDS compensation techniques are compared considering the unicast/broadcast mode (S.Ch. DFE and S.Ch. TDS in Fig. 5). The results indicate that with an SNR of 15 dB, both techniques yield to 10^{-7} BER, improving performance compared with OOK without compensation channel and nearly reaching the limits of OOK theory. However, contrary to DFE, the data rate of the TDS scheme is divided by the code size. Consequently, in this mode, the DFE configuration provides higher data rate with improved SNR compared to TDS and thus produces a good BER performance for the single channel access mode.

Secondly, the effectiveness of TDS in the parallel channel access mode was tested with the same channel interference used in previous analysis. Two and three parallel communications were configured to evaluate the system performance (2-P.Ch. and 3-P.Ch. TDS in Fig. 5). These configurations are representative for multiple-unicast, many-to-one and all-to-one communication patterns of the parallel mode for the network topology shown in Fig. 4. In both cases, the results highlight that the channel is compensated even though more than one transmitter is transmitting data at the same time. However, due to ADC limitations and Multiple Access Interference, the SNR increases by 1.5 dB and 2.5 dB compared with single channel access, respectively for two and three parallel channels. This parallel mode brings significant benefits in terms of communication energy and latency, compared to multiple single channel accesses on different time slots. The energy efficiency and the decrease in latency will perfectly scale with the number of clusters, which demonstrates the potential of our adaptive transceiver for a large number of cores.

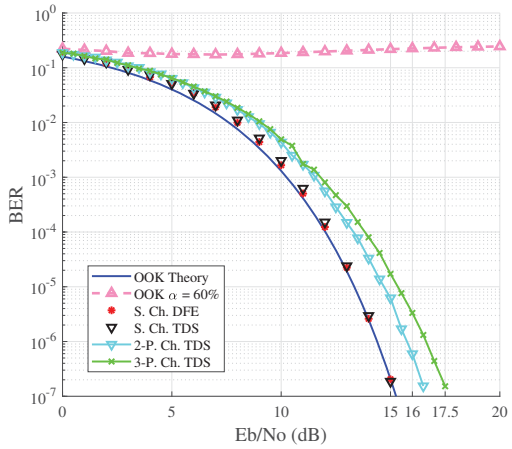

Fig. 5. Demodulation performance BER scaling according to SNR for the considered techniques with $\alpha = 60\%$.

B. Synthesis Results and Discussion

The architecture depicted in Fig. 3 has been synthesized from C/C++ using HLS and logic synthesis. Most elements are clocked at 1.25 GHz, except a low complexity SER(8:1) block that was designed at 10 GHz. Data interfaces with the router/switch have 32-bit width. Synthesis results of the blocks of the wireless interface are summarized in Table I. The total power consumption of each component reports both static and dynamic power consumed. Nevertheless, the static power represents less than 1% of the total power, mainly thanks to the 28-nm FDSOI low-leakage technology. Therefore, unused blocks after network configuration do not represent significant power consumption. The proposed WI consumes 3.27 mW and occupies 1556.41 $\mu\mathrm{m}^2$ for four clusters. These values consider all the elements corresponding to the architecture shown in Fig. 3, disregarding the RF, ADC and router/switch.

Based on [23], Table I also provides area and power for the ADC block and for a low-power OOK RF transceiver. The ADC block may be considered as a drawback in our architecture, since it consumes the bulk of area and power of the WI. However, any digital filter or channel compensation technique requires this block to perform corrections. The ADC architecture needed in this type of WiNoC is a parallel one, as mentioned in Section VI. This allows to decrease the frequency of digital filters and therefore to reduce power consumption.

Therefore, to push the performance limits of wireless links in WiNoC, the use of an ADC is mandatory. This opens for relevant research to build new ADC designs dedicated to the WiNoC context.

The proposed solution, which considers all mandatory elements into the digital WI part including the compensation techniques, represents less than 1% (10%) of the total WI area (power). Furthermore, the solution proposed in this paper improves by 67% the power consumption of the technique presented in [25] without any channel compensation. Moreover, our adaptive approach provides on-chip communication with a reliability near to the limit of the OOK theory, both for single unicast and parallel multicast/broadcast configurations.

TABLE I
SYNTHESIS RESULTS (AREA AND POWER CONSUMPTION) OF THE WIRELESS INTERFACE ARCHITECTURE USING 28-NM FDSOI.

WI Block	**Area** (μm^2)	**Power** (mW)
DSSS encoder	52	0.07
DFE block	7.34	0.0023
TDS decoder	93.69	0.11
Serializer 32:1:8 (1.25 Gbps)	270	0.27
Serializer 8:1(10 Gbps)	94	1.15
Deserializer 8:32-bit (1.25 Gbps)	189	0.33
Deserializer 1:32-bit (1.25 Gbps)	221	0.37
Total Adaptive WI ($N = 4$)	1556.41	3.27
4-bit ADC [23]	9000	16
OOK Transceiver [26], [27]	not specified	10

VIII. CONCLUSIONS

WiNoC communication technology is expected to overcome limitations of conventional wired communications. However, communication reliability through a realistic wireless channel still remains an unexplored area in the state of the art. Furthermore, due to, *e.g.*, the cache coherence protocols supported by on chip interconnection networks, various multicast/broadcast scenarios are important to be considered during the wireless interface design of WiNoCs. As a consequence, in this paper, we propose an adaptive digital transceiver using channel compensation techniques for single and multiple parallel channel access modes. Our study demonstrates the significant reliability improvement of an OOK scheme facing a channel with high dispersion.

The area (power) overhead of the adaptive digital transceiver for a four-cluster receiver is only $1556.41\mu m^2$ ($3.27mW$), which represents less than 1% (10%) of the wireless interface. Therefore, the gain in performance of our proposed scheme is significant at the cost of a very low area/power overhead. In addition, unlike an error-correcting code, our solution offers more throughput and less latency when the number of clusters sharing the wireless channel increases (parallel mode), as well as in unicast/broadcast mode.

REFERENCES

[1] S. Das *et al.*, "Energy-efficient and reliable 3D Network-on-Chip (NoC): Architectures and optimization algorithms," in *Proc. IEEE/ACM Inter. Conf. on Computer-Aided Design (ICCAD)*, 2016, pp. 1–6.

[2] A. Brière *et al.*, "A Dynamically Reconfigurable RF NoC for Many-Core," in *Proce. on Great Lakes Symposium on VLSI*, 2015, pp. 139–144. [Online]. Available: http://doi.acm.org/10.1145/2742060.2742082

[3] Z. Chen *et al.*, "A Power Efficient and Compact Optical Interconnect for Network-on-Chip," *IEEE Computer Arch. Letters*, vol. 13, no. 1, pp. 5–8, 2014.

[4] A. Mineo *et al.*, "Runtime Tunable Transmitting Power Technique in mm-Wave WiNoC Architectures," *IEEE Trans. on VLSI Systems*, vol. 24, no. 4, pp. 1535–1545, 2016.

[5] X. Yu *et al.*, "A wideband body-enabled millimeter-wave transceiver for wireless network-on-chip," in *Inter. Midwest Symposium on Circuits and Systems (MWSCAS)*, 2011, pp. 1–4.

[6] X. Yu, H. Rashtian *et al.*, "An 18.7-Gb/s 60-GHz OOK Demodulator in 65-nm CMOS for Wireless Network-on-Chip," *IEEE Trans. on Circuits and Systems I: Regular Papers*, vol. 62, no. 3, pp. 799–806, 2015.

[7] P. P. Pande *et al.*, "Hybrid wireless network on chip: A new paradigm in multi-core design," in *Proc. Int. Work. on Network on Chip Arch.*, 2009, pp. 71–76.

[8] A. Asaduzzaman *et al.*, "An Energy-Efficient Directory Based Multicore Architecture with Wireless Routers to Minimize the Communication Latency," *IEEE Trans. on Parallel and Distributed Sys.*, vol. 28, no. 2, pp. 374–385, 2017.

[9] D. Zhao *et al.*, "Design of Multi-channel Wireless NoC to Improve On-chip Communication Capacity," in *Proc. IEEE Int. Symp. on NoC*, 2011, pp. 177–184.

[10] S.-B. Lee *et al.*, "A Scalable Micro Wireless Interconnect Structure for CMPs," in *Proc. Int. Conf. on Mobile Computing and Networking*, 2009, pp. 217–228.

[11] S. H. Gade, S. Garg, and S. Deb, "OFDM Based High Data Rate, Fading Resilient Transceiver for Wireless Networks-on-Chip," in *Proc. IEEE Computer Society Annual Symp. on VLSI (ISVLSI)*, 2017, pp. 483–488.

[12] A. Vidapalapati *et al.*, "NoC architectures with adaptive CDMA based wireless links," in *Proc. IEEE Inter. Symp. on Circuits and Systems*, 2012, pp. 636–639.

[13] D. W. Matolak *et al.*, "Channel modeling for wireless networks-on-chips," *IEEE Comm. Magazine*, vol. 51, no. 6, pp. 180–186, 2013.

[14] M. O. Agyeman *et al.*, "An Analytical Channel Model for Emerging Wireless Networks-on-Chip," in *Proc. IEEE Int. Conf. on Comp. Science and Engineering (CSE)*, 2016, pp. 9–15.

[15] I. E. Masri *et al.*, "Integrated dipole antennas and propagation channel on silicon in Ka band for WiNoC applications," in *Proc. IEEE Work. on Signal and Power Integrity (SPI)*, 2018, pp. 1–4.

[16] A. Sikder *et al.*, "Reconfigurable Optical and Wireless (R-OWN) Network-on-Chip for High Performance Computing," in *Proc. ACM Intern. Conf. on Nanoscale Comp. and Comm.*, 2016, pp. 25:1–25:6.

[17] V. Catania, A. Mineo, S. Monteleone, M. Palesi, and D. Patti, "Improving Energy Efficiency in Wireless Network-on-Chip Architectures," *J. Emerg. Technol. Comput. Syst.*, vol. 14, no. 1, pp. 9:1–9:24, 2017.

[18] K. Kim *et al.*, "A plane wave model approach to understanding propagation in an intra-chip communication system," in *Proc. IEEE Ant. and Propag. Society Int. Symp. Digest*, 2001, pp. 166–169, vol.2.

[19] Y. P. Zhang *et al.*, "Propagation Mechanisms of Radio Waves Over Intra-Chip Channels With Integrated Antennas: Frequency-Domain Measurements and Time-Domain Analysis," *IEEE Trans. on Ant. and Prop.*, vol. 55, no. 10, pp. 2900–2906, 2007.

[20] J. O. Sosa, O. Sentieys, and C. Roland, "A Diversity Scheme to Enhance the Reliability of Wireless NoC in Multipath Channel Environment," in *Int. Symp. on Network-on-Chip (NOCS)*, 2018, pp. 1–8.

[21] Proakis, *Digital Communications 5th Edition*. McGraw Hill, 2007.

[22] A. Spalvieri and M. Magarini, "Computing the feedback filter of the decision feedback equalizer at the fft speed," in *Asilomar Conf. on Signals, Systems and Computers*, 2004, pp. 804–808, vol.1.

[23] S. L. Tual *et al.*, "22.3 A 20GHz-BW 6b 10GS/s 32mW time-interleaved SAR ADC with Master T&H in 28nm UTBB FDSOI technology," in *Proc. IEEE Inter. Solid-State Circuits Conf. (ISSCC)*, 2014, pp. 382–383.

[24] K. Chang *et al.*, "Performance evaluation and design trade-offs for wireless network-on-chip architectures," *Journal on Emerg. Technol. in Computing Systems (JETC)*, vol. 8, no. 3, pp. 23:1–23:25, 2012.

[25] S. Deb *et al.*, "Enhancing performance of network-on-chip architectures with millimeter-wave wireless interconnects," in *IEEE Int. Conf. on Appli.-Specific Sys., Archi. and Processors (ASAP)*, 2010, pp. 73–80.

[26] T. Shinde *et al.*, "A 0.24pJ/Bit, 16Gbps OOK Transmitter Circuit in 45-nm CMOS for Inter and Intra-Chip Wireless Interconnects," in *Proc. Great Lakes Symp. on VLSI (GLVLSI)*, 2018, pp. 69–74.

[27] S. Subramaniam *et al.*, "A 0.36pJ/bit, 17Gbps OOK receiver in 45-nm CMOS for inter and intra-chip wireless interconnects," in *IEEE Int. System-on-Chip Conf. (SOCC)*, 2017, pp. 132–137.