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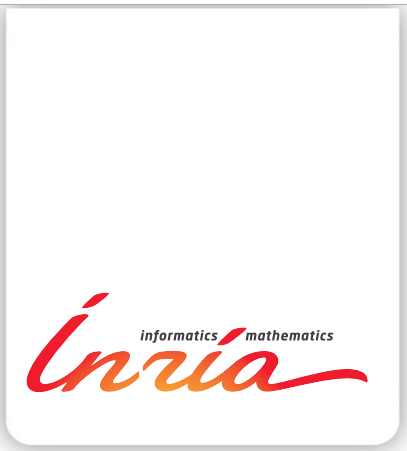

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Abstract: This report presents VLSAT-3 (an acronym for "Very Large Boolean SATisfiability problems"), the third part of a benchmark suite to be used in scientific experiments and software competitions addressing SAT and SMT (Satisfiability Modulo Theories) solving issues. VLSAT-3 contains 1200 (600 satisfiable and 600 unsatisfiable) quantifier-free first-order logic formulas of increasing complexity, proposed in SMT-LIB format under a permissive Creative Commons license. More than 90% of these benchmarks have been used during the 16$^{\text{th}}$ International Satisfiability Modulo Theories Competition (SMT-COMP 2021).

Key-words: benchmark suite, data set, SMT-LIB, Nested-Unit Petri Net, NUPN, Petri Net, Satisfiability Modulo Theories, SMT formula, SMT solver

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Le jeu de tests VLSAT-3

Résumé : VLSAT-3 (acronyme anglais de "très grands problèmes de satisfaisabilité booléenne") est le troisième volet d'une suite de tests destinée aux expérimentations scientifiques et aux compétitions de logiciels pour la résolution de problèmes SAT et SMT (Satisfaisabilité Modulo des Théories). VLSAT-3 contient 1200 formules logiques (600 satisfaisables et 600 insatisfaisables) du premier ordre sans quantificateur, de complexité croissante, fournies en format SMT-LIB sous une licence Creative Commons permissive. Plus de 90% de ces tests ont été utilisés lors de la $16^{\text{ème}}$ Compétition Internationale de Satisfaisabilité Modulo des Théories (SMT-COMP 2021).

Mots-clés : ensemble de données, formule SMT, Nested-Unit Petri Net, NUPN, réseau de Petri, résolveur SMT, satisfaisabilité modulo des théories, SMT-LIB, suite de tests

1 Benchmark Description

We previously published two test suites, named VLSAT-1 [2] and VLSAT-2 [3], containing SAT formulas. VLSAT-3[1] is a collection of 1200 SMT (Satisfiability Modulo Theories) formulas (i.e., first-order logic formulas), written in six different quantifier-free logic fragments. For each of these logic fragments, 100 satisfiable and 100 unsatisfiable formulas are provided, which results in 12 families containing 100 benchmarks each.

Each formula is provided as a separate file, encoded in the SMT-LIB 2.6 format [1]. Each file is then compressed using bzip2 to save disk space and allow faster downloads. The 1200 formulas require 2.4 gigabytes of disk space and 132 megabytes when compressed using bzip2.

2 Scientific Context

Interesting SMT formulas can be generated as a by-product of our recent work [4] on the decomposition of Petri nets into networks of automata, a problem that has been around since the early 70s. Concretely, we developed a tool chain that takes as input a Petri net (which must be ordinary, safe, and hopefully not too large) and produces as output a network of automata that execute concurrently and synchronize using shared transitions. Precisely, this network is expressed as a *Nested-Unit Petri Net* (NUPN) [5], i.e., an extension of a Petri net, in which places are grouped into sets (called *units*) that denote sequential components. A NUPN provides a proper structuring of its underlying Petri net, and enables formal verification tools to be more efficient in terms of memory and CPU time. Hence, the NUPN concept has been implemented in many tools and adopted by software competitions, such as the Model Checking Contest[3] [9, 8] and the Rigorous Examination of Reactive Systems challenge[4] [6, 10, 7]. Each NUPN generated by our tool chain is *flat*, meaning that its units are not recursively nested in each other, and *unit-safe*, meaning that each unit has at most one execution token at a time.

Our tool chain works by reformulating concurrency constraints on Petri nets as logical problems, which can be later solved using third-party software, such as SAT solvers, SMT solvers, and tools for graph coloring and finding maximum cliques, depending on the chosen strategy [4]. When a strategy involving SMT solving is selected, the tool chain produces formulas to be processed by SMT solvers. The tool chain is solver-agnostic and supports six standard SMT logic fragments.

3 Structure of Formulas

Each of our formulas was produced for a particular Petri net. A formula depends on four factors:

- the set P of the places of the Petri net;
- a *concurrency relation* $\parallel$ defined over P, such that $p \parallel p'$ iff both places p and p' may simultaneously have an execution token;

[1] `https://cadp.inria.fr/resources/vlsat/3.html`
[2] License terms available from `http://creativecommons.org/licenses/by/4.0`
[3] `https://mcc.lip6.fr`
[4] `http://rers-challenge.org`

- a chosen number n of units; and
- a chosen SMT logic fragment, among QF_BV, QF_DT, QF_IDL, QF_UFBV, QF_UFDT, and QF_UFIDL.

A formula checks whether there exists a partition of P into n subsets P_i $(1 \leq i \leq n)$ such that, for each i, and for any two places p and p' of P_i, $p \neq p' \Longrightarrow \neg\,(p \parallel p')$. A model of this formula is thus an allocation of places into n leaf units, i.e., a valid decomposition of the Petri net. This can also be seen as an instance of the graph coloring problem, in which n colors are to be used for the graph with vertices defined by the places of P and edges defined by the concurrency relation. A formula is only satisfiable if the value of n is large enough (namely, greater than or equal to the chromatic number of the graph), so that at least one decomposition exists.

Notice that if a decomposition having n units exists, it is possible to generate $n! - 1$ another similar decompositions, just by permuting unit numbers. Thus, instead of adding constraints in the formulas to express that each place p belongs to some unit of $1 \ldots n$, we break the symmetry between units by constraining each place p to belongs some unit of $1 \ldots \min(p, n)$.

More precisely, each formula is generated as follows, depending on the chosen logic fragment:

- The QF_BV fragment corresponds to *quantifier-free bit-vector* logic. It supports fixed-size Boolean vectors, as well as logical, relational, and arithmetical operators on these vectors. Our encoding for QF_BV creates, for each place p, a bit vector b_p of length n such that $b_p[u]$ is true iff place p can belong to unit u. Then, to prevent concurrent places being assigned in the same unit, the following constraint is added: for each pair of places (p_1, p_2) such that $(p_1 \parallel p_2) \wedge (p_1 < p_2)$, b_{p_1} & $b_{p_2} = 0_{(n)}$, where "&" denotes the bitwise "and" operator, and "$0_{(n)}$" denotes the zero vector of size n. Finally, for each place p, we add the following symmetry-breaking constraint to express that p belongs to at least one unit: $\bigvee_{1 \leq u \leq \min(p,n)} (b_p[1:u] \neq 0_{(u)})$, where $[i:j]$ denotes the operator that extracts, from a vector, the i^{th} bit to the j^{th}. Notice that there is no constraint requiring that each place belongs to one single unit. Thus, the model returned by the SMT solver may not be a partition of P. Yet, having a partition is necessary to produce a valid decomposition of the Petri net into a flat NUPN. To do so, any model that is not a partition is transformed into a partition using the first-fit-decreasing bin-packing algorithm described in [4].
- The QF_UFBV fragment corresponds to *quantifier-free uninterpreted-function bit-vector* logic. The *uninterpreted function* theory enables the declaration of function symbols, which are given only by their signatures (i.e., the types of their arguments and results). Our encoding for QF_UFBV is based on that of QF_BV but, instead of the b_p variables, we define an uninterpreted function u from the set of bitvectors of size $\lceil \log_2(\text{card}\,(P)) \rceil$ to the set of bitvectors of size n, each occurrence of b_p being replaced with $u(\lambda(\#p))$ in the constraints, where $\#p$ is a bijection from places numbers to the interval $1 \ldots \text{card}\,(P)$, and where λ is an injection from $1 \ldots \text{card}\,(P)$ to the set of bitvectors of size $\lceil \log_2(\text{card}\,(P)) \rceil$.
- The QF_DT fragment corresponds to *quantifier-free data-type* logic. It supports the definition of algebraic data types, such as enumerated types, records, lists, trees, etc. Our encoding for QF_DT defines an enumerated type *Unit*, which contains one value per unit. Our encoding also creates, for each place p, one variable x_p of type *Unit*. Then, to prevent concurrent places being assigned to the same unit, the following constraint is added: for each pair of places (p_1, p_2) such that $(p_1 \parallel p_2) \wedge (p_1 < p_2)$, $x_{p_1} \neq x_{p_2}$. Finally, the symmetry is broken by adding, for each variable x_p whose place number $\#p$ is less than n, the constraint $\bigvee_{1 \leq u \leq p} (x_p = u)$.

- The QF_UFDT fragment corresponds to *quantifier-free uninterpreted-function data-type* logic. Our encoding for QF_UFDT is based on that of QF_DT but, instead of the x_p variables, defines both an enumerated type *Place*, which contains one value per place, and an uninterpreted function $u : \mathit{Place} \mapsto \mathit{Unit}$, each occurrence of x_p being replaced with $u(p)$ in the constraints.
- The QF_IDL fragment corresponds to *quantifier-free integer-difference* logic. It supports integer variables and arithmetic constraints on the difference between two variables. The *integer difference logic* theory provides integers, which can also have constraints of the form $(x - y)$ *op* c, where x is an integer variable, y is either an integer variable or a constant, *op* is a comparison operator, and c is an integer constant. Our encoding for QF_IDL is based on that of QF_DT but declares the variables x_p to be of Integer type instead of *Unit*. Since integers are unbounded, each variable x_p whose place number $\#p$ is greater or equal than n must be constrained by adding $\bigvee_{1 \leq u \leq n}(x_p = u)$, since x_p is not subject to a symmetry-break constraint. Notice that we could replace some disjunctive clauses with difference constraints (e.g., $x_3 = 1 \vee x_3 = 2 \vee x_3 = 3$ being replaced with $0 \leq x_3 \leq 3$); this variant was tried, but found to be slower during our early experiments using the Z3 solver, and therefore, not used later.
- The QF_UFIDL fragment corresponds to *quantifier-free uninterpreted-function integer-difference* logic. Our encoding for QF_UFIDL is based on that of QF_IDL, with the same changes as for evolving from QF_BV to QF_UFBV.

4 Selection of Benchmarks

We applied our approach to a large collection of more than 12,000 Petri nets from multiple sources, many of which are related to industrial problems, such as communication protocols, distributed systems, and hardware circuits. We thus generated a large collection of more than 51,000 SMT formulas produced by our tool chain. In this collection, we carefully selected a subset of formulas matching the requirements of the 16$^{\text{th}}$ International Satisfiability Modulo Theories Competition (SMT-COMP 2021)[5].

For our experiments, we used six state-of-the-art solvers: Boolector 3.2.0 (compiled with its "--only-cadical" option), Bitwuzla (the version submitted to the SMT-COMP 2020), CVC4 1.8, MathSAT 5.6.5, Yices 2.6.2, and Z3 4.8.9. These include all the solvers that participated in SMT-COMP 2019 and/or in SMT-COMP 2020 and have been the fastest or the second fastest for any logic fragment supported by our toolchain (i.e., Boolector, Bitwuzla, CVC4, Yices, and Z3), as well as the solvers used for constructing VLSAT-2 [3] and that can solve both SAT and SMT formulas (i.e., MathSAT and Z3).

For each formula ϕ, let $\min(\phi)$ the smallest execution time measured among all the six selected solvers, using a Linux server equipped with a Xeon E5-2630 v3 and 128 GB RAM. We selected the 46,000+ formulas ϕ such that $\min(\phi)$ ranges between 10 seconds and 1 hour. For each of the six supported logic fragments, we created one family of satisfiable formulas and one family of unsatisfiable formulas. We partitioned each family in (at most) 60 classes, by gathering in the same class all formulas ϕ having the same $\min(\phi)$ rounded to the nearest minute. Finally, in each class, we selected a few formulas having a low complexity (measured in terms of SMT-LIB file size), and took the same number (plus or minus one) of formulas in each class, until reaching 100 formulas per family.

[5] https://smt-comp.github.io/2021/

5 Resulting Benchmarks

The 12 families of the VLSAT-3 benchmark suite are listed in Table 1, the columns of which have the following meaning:

- Column 1: Letter identifying the corresponding family of formulas.
- Column 2: Satisfiability (SAT or UNSAT); all formulas in a given family have the same satisfiability.
- Column 3: One out of six quantifier-free first-order logic fragment; all formulas in a given family are in the same logic fragment.
- Column 4: Percentage of the formulas in this family that have been selected by the organizers of SMT-COMP 2021.
- Column 5: Percentage of the formulas in this family among all the benchmarks of the corresponding logic in the Single Query Track (SQT) of SMT-COMP 2021.
- Column 6: Percentage of the formulas in this family among all the benchmarks of the corresponding logic in the Model Validation Track (MVT) of SMT-COMP 2021.
- Column 7: Percentage of the formulas in this family among all the benchmarks of the corresponding logic in the Unsat Core Track (UCT) of SMT-COMP 2021.

family	satisfiability	logic	selection	SQT share	MVT share	UCT share
a	UNSAT	QF_BV	76 %	0.86 %		2.65 %
b		QF_DT	100 %	49.02 %		100 %
c		QF_IDL	100 %	8.79 %		100 %
d		QF_UFBV	88 %	29.33 %		30.67 %
e		QF_UFDT	100 %	49.26 %		100 %
f		QF_UFIDL	100 %	33.33 %		88.50 %
g	SAT	QF_BV	76 %	0.86 %	1.05 %	
h		QF_DT	100 %	49.02 %		
i		QF_IDL	70 %	6.15 %	10.13 %	
j		QF_UFBV	81 %	27.0 %	21.6 %	
k		QF_UFDT	100 %	49.26 %		
l		QF_UFIDL	100 %	33.33 %	48.54 %	

Table 1: List of the 12 families of VLSAT-3 formulas

In a nutshell, 90.9 % of the VLSAT-3 benchmarks have been used by the organizers of SMT-COMP 2021. Additionally, 7.8 % of the benchmarks of the Single Query Track, 2.9 % of the benchmarks of the Model Validation Track, and 14.0 % of the benchmarks of the Unsat Core Track are VLSAT-3 benchmarks.

We now provide 12 tables that describe each family in detail. The first one, Table 2, corresponds to family “a”, and the last one, Table 13, corresponds to family “l”.

Each row of a table corresponds to one benchmark. The columns of these tables contain the following data:

- Column name: Benchmark name, of the form "vlsat3_Fnn.smt2.bz2", where F is the family letter, and nn is a two-digit number ranging from 00 to 99.
- Column #variables (for QF_BV, QF_DT, and QF_IDL): Number of variables declared in the formula.
- Column card (for QF_BV, QF_DT, and QF_IDL): Cardinality of the type of all variables declared in the formula (or ∞ if the type has an infinite set of values).
- Column card_{in}: (for QF_UFBV, QF_UFDT, and QF_UFIDL): Cardinality of the domain of the uninterpreted function present in the formula (or ∞ if the domain is infinite).
- Column card_{out}: (for QF_UFBV, QF_UFDT, and QF_UFIDL): Cardinality of the codomain of the uninterpreted function present in the formula (or ∞ if the codomain is infinite).
- Column #asserts: Number of assertions in the formula.
- Column #ops: Number of operators in the formula.

Acknowledgements

The experiments presented in this paper were carried out using the Grid'5000[6] testbed, supported by a scientific interest group hosted by Inria and including Cnrs, Renater and several universities as well as other organizations.

[6] https://www.grid5000.fr

Table 2: Family "a": List of unsatisfiable VLSAT-3 formulas written in QF_BV logic

name	#variables	card	#asserts	#ops
a00	56	2^{11}	1463	7283
a01	80	2^{11}	3050	15,170
a02	80	2^{17}	3050	15,218
a03	56	2^{12}	1463	7291
a04	120	2^{15}	6975	34,747
a05	140	2^{17}	8750	43,598
a06	80	2^{18}	3050	15,226
a07	122	2^{11}	6963	34,651
a08	244	2^{10}	16,134	80,254
a09	80	2^{12}	3050	15,178
a10	112	2^{11}	6064	30,176
a11	164	2^{11}	13,172	65,612
a12	60	2^{15}	1407	7027
a13	80	2^{16}	3050	15,210
a14	138	2^{11}	9282	46,214
a15	48	2^{23}	1113	5645
a16	56	2^{16}	1463	7323
a17	84	2^{12}	1819	9015
a18	87	2^{14}	3180	15,830
a19	123	2^{15}	5120	25,466
a20	141	2^{11}	6054	30,068
a21	87	2^{14}	2672	13,290
a22	101	2^{19}	3524	17,562
a23	120	2^{16}	6975	34,755
a24	70	2^{17}	1633	8153
a25	77	2^{16}	1907	9501
a26	118	2^{15}	4995	24,851
a27	43	2^{15}	591	2981
a28	99	2^{11}	4081	20,287
a29	128	2^{11}	4185	20,749
a30	56	2^{13}	1463	7299
a31	85	2^{14}	2077	10,319
a32	87	2^{19}	2672	13,330
a33	139	2^{11}	5667	28,137
a34	161	2^{11}	6337	31,443
a35	155	2^{14}	9328	46,434
a36	61	2^{15}	1248	6230
a37	78	2^{13}	2162	10,750
a38	168	2^{20}	8560	42,616
a39	44	2^{25}	946	4834
a40	130	2^{15}	6171	30,707
a41	224	2^{13}	15,832	78,808
a42	237	2^{14}	18,611	92,685
a43	28	2^{11}	224	1144
a44	58	2^{16}	1555	7779
a45	139	2^{11}	5449	27,047
a46	233	2^{15}	20,436	101,826
a47	45	2^{14}	679	3409
a48	54	2^{16}	928	4652
a49	62	2^{30}	1849	9353

name	#variables	card	#asserts	#ops
a50	140	2^{19}	8750	43,614
a51	114	2^{11}	2465	12,177
a52	90	2^{18}	2808	13,996
a53	118	2^{18}	6333	31,565
a54	176	2^{11}	12,053	59,993
a55	47	2^{16}	745	3751
a56	57	2^{13}	1306	6512
a57	106	2^{11}	4140	20,568
a58	190	2^{15}	13,177	65,617
a59	80	2^{13}	3050	15,186
a60	145	2^{13}	4258	21,096
a61	418	2^{11}	76,832	383,404
a62	274	2^{12}	30,943	154,255
a63	321	2^{11}	46,286	230,868
a64	387	2^{11}	61,385	306,231
a65	409	2^{11}	76,216	380,342
a66	372	2^{11}	65,248	325,576
a67	739	2^{11}	263,743	1,317,317
a68	57	2^{12}	1306	6504
a69	95	2^{12}	4076	20,278
a70	143	2^{48}	9242	46,300
a71	187	2^{13}	15,773	78,587
a72	64	2^{14}	2003	9991
a73	94	2^{12}	4007	19,935
a74	214	2^{13}	16,183	80,583
a75	341	2^{12}	21,828	108,546
a76	124	2^{11}	3938	19,522
a77	280	2^{13}	37,240	185,736
a78	80	2^{11}	1642	8130
a79	115	2^{12}	5325	26,483
a80	279	2^{11}	33,589	167,467
a81	379	2^{11}	36,702	182,832
a82	438	2^{11}	89,288	445,644
a83	74	2^{14}	1048	5196
a84	513	2^{11}	119,974	598,924
a85	73	2^{14}	1136	5638
a86	549	2^{11}	70,640	352,182
a87	455	2^{11}	95,112	474,730
a88	519	2^{11}	63,046	314,272
a89	398	2^{11}	74,088	369,724
a90	589	2^{11}	83,903	418,417
a91	444	2^{11}	90,479	451,587
a92	374	2^{11}	44,026	219,462
a93	482	2^{11}	107,271	535,471
a94	588	2^{11}	144,272	720,264
a95	236	2^{11}	23,702	118,118
a96	342	2^{11}	50,614	252,466
a97	440	2^{121}	91,418	457,170
a98	318	2^{11}	34,220	170,544
a99	202	2^{11}	16,451	81,931

Table 3: Family "b": List of unsatisfiable VLSAT-3 formulas written in QF_DT logic

name	#variables	card	#asserts	#ops
b00	56	16	1422	4504
b01	164	11	13,018	39,162
b02	56	12	1418	4384
b03	120	16	6870	20,848
b04	118	14	4890	14,850
b05	140	18	8627	26,185
b06	155	13	9185	27,709
b07	48	21	1085	3673
b08	161	11	6186	18,666
b09	228	11	25,444	76,440
b10	56	17	1423	4539
b11	122	11	3633	11,007
b12	120	17	6871	20,883
b13	72	13	1947	5995
b14	80	17	2986	9228
b15	249	15	23,529	70,795
b16	168	20	8411	25,611
b17	155	14	9186	27,738
b18	192	11	9254	27,870
b19	70	15	1577	4939
b20	71	11	1859	5685
b21	80	13	2982	9100
b22	137	11	4890	14,778
b23	112	12	5963	18,019
b24	231	11	17,648	53,052
b25	56	13	1419	4411
b26	220	15	15,636	47,116
b27	366	11	33,082	99,354
b28	95	14	2688	8244
b29	101	19	3441	10,663
b30	164	12	13,019	39,187
b31	124	14	5446	16,518
b32	140	19	8628	26,224
b33	174	21	9097	27,709
b34	72	14	1948	6024
b35	124	11	3797	11,499
b36	118	15	4891	14,881
b37	250	11	16,203	48,717
b38	265	11	23,486	70,566
b39	318	11	33,912	101,844
b40	36	14	387	1341
b41	128	11	4067	12,309
b42	643	17	27,546	82,908
b43	244	11	15,900	47,808
b44	228	12	25,445	76,465
b45	262	12	33,713	101,269
b46	132	12	8072	24,346
b47	182	11	8875	26,733
b48	313	11	26,245	78,843
b49	48	22	1086	3718

name	#variables	card	#asserts	#ops
b50	74	13	1844	5686
b51	141	11	5923	17,877
b52	187	11	8484	25,560
b53	163	14	9451	28,533
b54	263	11	18,641	56,031
b55	108	11	2849	8655
b56	80	19	2988	9304
b57	173	11	4966	15,006
b58	259	11	16,567	49,809
b59	290	12	33,862	101,716
b60	312	14	34,861	104,763
b61	100	11	2539	7725
b62	182	12	15,492	46,606
b63	197	12	17,102	51,436
b64	121	12	4860	14,710
b65	146	12	9804	29,542
b66	218	12	22,476	67,558
b67	137	21	7951	24,271
b68	272	11	18,181	54,651
b69	266	12	33,804	101,542
b70	140	12	7273	21,949
b71	142	12	9392	28,306
b72	154	12	11,085	33,385
b73	196	12	18,722	56,296
b74	265	11	23,519	70,665
b75	271	12	33,783	101,479
b76	112	12	5732	17,326
b77	161	17	11,412	34,506
b78	287	12	34,877	104,761
b79	735	83	265,952	804,660
b80	735	84	265,953	804,829
b81	845	11	207,417	622,359
b82	236	11	23,476	70,536
b83	575	145	156,823	491,347
b84	735	85	265,954	805,000
b85	575	144	156,822	491,056
b86	575	146	156,824	491,640
b87	575	147	156,825	491,935
b88	575	148	156,826	492,232
b89	735	86	265,955	805,173
b90	609	11	149,949	449,955
b91	735	89	265,958	805,704
b92	242	12	23,786	71,488
b93	575	150	156,828	492,832
b94	48	31	1065	4123
b95	1026	46	404,855	1,216,633
b96	575	149	156,827	492,531
b97	1016	81	509,749	1,535,725
b98	1019	81	512,764	1,544,770
b99	717	205	249,677	790,849

Table 4: Family "c": List of unsatisfiable VLSAT-3 formulas written in QF_IDL logic

name	#variables	card	#asserts	#ops
c00	56	∞	1463	5687
c01	80	∞	3050	10,936
c02	215	∞	19,420	61,226
c03	216	∞	23,436	117,176
c04	56	∞	1463	5773
c05	80	∞	3050	11,072
c06	80	∞	3050	11,206
c07	194	∞	18,871	67,709
c08	84	∞	1819	7765
c09	80	∞	3050	11,338
c10	124	∞	5557	20,397
c11	194	∞	18,871	68,359
c12	56	∞	1463	5857
c13	112	∞	6064	21,144
c14	132	∞	8193	28,091
c15	164	∞	13,172	43,924
c16	56	∞	1463	6019
c17	136	∞	8792	32,796
c18	366	∞	33,438	108,254
c19	262	∞	33,964	108,546
c20	56	∞	1463	5939
c21	87	∞	3180	12,082
c22	141	∞	6054	21,412
c23	161	∞	6337	23,039
c24	71	∞	1920	7448
c25	137	∞	8068	27,358
c26	166	∞	13,507	44,985
c27	325	∞	15,332	53,662
c28	84	∞	1819	7903
c29	244	∞	16,134	54,124
c30	366	∞	33,438	108,964
c31	262	∞	33,964	109,044
c32	80	∞	3050	11,468
c33	142	∞	9523	32,361
c34	265	∞	23,741	77,449
c35	228	∞	25,662	83,186
c36	137	∞	8068	27,608
c37	137	∞	8068	29,066
c38	285	∞	20,436	68,014
c39	228	∞	25,662	83,614
c40	226	∞	14,011	47,751
c41	215	∞	18,071	61,249
c42	285	∞	20,436	68,560
c43	289	∞	21,221	70,465
c44	139	∞	5667	20,709
c45	112	∞	6064	21,340
c46	231	∞	17,869	59,455
c47	289	∞	21,221	71,019
c48	60	∞	1407	5987
c49	164	∞	13,172	44,224

name	#variables	card	#asserts	#ops
c50	272	∞	18,443	62,243
c51	297	∞	22,683	75,613
c52	80	∞	3050	11,596
c53	120	∞	6975	24,523
c54	136	∞	8792	33,016
c55	247	∞	15,746	53,502
c56	55	∞	1026	4750
c57	118	∞	4995	18,723
c58	137	∞	8068	27,856
c59	198	∞	11,362	39,076
c60	47	∞	688	3388
c61	168	∞	8560	31,420
c62	240	∞	13,924	48,308
c63	306	∞	24,224	80,470
c64	42	∞	599	2951
c65	45	∞	680	3352
c66	142	∞	4788	18,156
c67	142	∞	9523	32,617
c68	74	∞	1906	7844
c69	161	∞	6337	23,335
c70	166	∞	13,507	45,289
c71	244	∞	16,134	54,588
c72	265	∞	23,741	77,955
c73	75	∞	1805	7691
c74	83	∞	2524	10,120
c75	128	∞	5689	21,145
c76	325	∞	15,332	54,912
c77	352	∞	52,053	163,107
c78	28	∞	224	1272
c79	54	∞	918	4390
c80	129	∞	2615	11,273
c81	148	∞	5549	20,337
c82	152	∞	10,953	37,207
c83	48	∞	754	3620
c84	250	∞	16,443	55,671
c85	321	∞	46,286	145,186
c86	342	∞	50,614	158,590
c87	622	∞	192,992	591,324
c88	57	∞	1306	5330
c89	113	∞	4010	15,598
c90	96	∞	3125	12,523
c91	176	∞	9488	34,808
c92	61	∞	1248	5632
c93	508	∞	89,854	284,590
c94	520	∞	135,460	677,296
c95	52	∞	1321	5527
c96	40	∞	793	3511
c97	118	∞	3673	14,347
c98	67	∞	1245	5839
c99	159	∞	5105	19,583

Table 5: Family "d": List of unsatisfiable VLSAT-3 formulas written in QF_UFBV logic

name	card_{in}	card_{out}	#asserts	#ops
d00	2^{7}	2^{17}	3050	21,142
d01	2^{8}	2^{14}	8576	59,647
d02	2^{7}	2^{16}	6975	48,495
d03	2^{8}	2^{15}	8576	59,649
d04	2^{7}	2^{12}	1819	12,503
d05	2^{7}	2^{19}	3050	21,146
d06	2^{6}	2^{13}	1407	9693
d07	2^{6}	2^{16}	1463	10,103
d08	2^{7}	2^{11}	5833	40,515
d09	2^{8}	2^{11}	9282	64,580
d10	2^{6}	2^{13}	1463	10,097
d11	2^{8}	2^{11}	9523	66,255
d12	2^{7}	2^{13}	3050	21,134
d13	2^{8}	2^{11}	13,507	94,071
d14	2^{7}	2^{12}	3050	21,132
d15	2^{8}	2^{11}	11,362	78,960
d16	2^{6}	2^{15}	1463	10,101
d17	2^{7}	2^{13}	1819	12,505
d18	2^{6}	2^{13}	1306	8995
d19	2^{7}	2^{14}	1487	10,240
d20	2^{7}	2^{16}	3050	21,140
d21	2^{7}	2^{14}	5557	38,553
d22	2^{7}	2^{13}	3180	22,023
d23	2^{8}	2^{21}	9488	65,928
d24	2^{8}	2^{11}	4788	33,110
d25	2^{8}	2^{10}	5667	39,270
d26	2^{6}	2^{14}	688	4701
d27	2^{8}	2^{17}	8750	60,862
d28	2^{7}	2^{15}	3050	21,138
d29	2^{8}	2^{12}	15,832	110,174
d30	2^{7}	2^{15}	1892	13,041
d31	2^{7}	2^{18}	3050	21,144
d32	2^{8}	2^{11}	6337	43,896
d33	2^{8}	2^{11}	13,924	96,768
d34	2^{7}	2^{13}	4995	34,635
d35	2^{8}	2^{16}	8576	59,651
d36	2^{7}	2^{11}	3083	21,271
d37	2^{7}	2^{15}	6975	48,493
d38	2^{7}	2^{15}	1811	12,477
d39	2^{8}	2^{20}	9488	65,926
d40	2^{7}	2^{13}	2672	18,467
d41	2^{7}	2^{16}	3125	21,617
d42	2^{6}	2^{29}	1140	7892
d43	2^{7}	2^{11}	4007	27,787
d44	2^{6}	2^{12}	679	4640
d45	2^{8}	2^{20}	8068	56,103
d46	2^{6}	2^{14}	396	2693
d47	2^{6}	2^{13}	578	3968
d48	2^{7}	2^{24}	4346	30,180
d49	2^{8}	2^{14}	12,108	84,137

name	card_{in}	card_{out}	#asserts	#ops
d50	2^{7}	2^{13}	2508	17,319
d51	2^{8}	2^{13}	7304	50,723
d52	2^{6}	2^{13}	591	4032
d53	2^{7}	2^{12}	3741	25,891
d54	2^{6}	2^{21}	1113	7687
d55	2^{6}	2^{24}	1506	10,423
d56	2^{7}	2^{13}	6363	44,223
d57	2^{5}	2^{10}	143	953
d58	2^{7}	2^{10}	551	3734
d59	2^{8}	2^{10}	4685	32,333
d60	2^{7}	2^{11}	2609	17,962
d61	2^{8}	2^{11}	18,157	126,483
d62	2^{9}	2^{10}	100,629	702,915
d63	2^{7}	2^{11}	6064	42,132
d64	2^{8}	2^{11}	10,023	69,725
d65	2^{8}	2^{11}	13,813	96,093
d66	2^{6}	2^{14}	585	4001
d67	2^{8}	2^{11}	17,483	121,807
d68	2^{9}	2^{10}	59,070	412,341
d69	2^{6}	2^{13}	1321	9115
d70	2^{9}	2^{11}	58,589	408,976
d71	2^{8}	2^{11}	17,079	118,979
d72	2^{8}	2^{11}	18,431	128,419
d73	2^{8}	2^{10}	22,645	157,849
d74	2^{7}	2^{10}	2840	19,577
d75	2^{6}	2^{13}	686	4688
d76	2^{9}	2^{11}	52,979	369,892
d77	2^{9}	2^{10}	93,919	656,005
d78	2^{6}	2^{12}	754	5156
d79	2^{7}	2^{10}	1971	13,551
d80	2^{7}	2^{11}	4803	33,335
d81	2^{6}	2^{13}	599	4091
d82	2^{7}	2^{19}	1778	12,299
d83	2^{6}	2^{15}	946	6518
d84	2^{7}	2^{11}	5325	36,950
d85	2^{8}	2^{10}	8768	60,959
d86	2^{10}	2^{10}	160,338	1,119,945
d87	2^{7}	2^{13}	2933	20,324
d88	2^{7}	2^{12}	3801	26,320
d89	2^{7}	2^{12}	3285	22,741
d90	2^{7}	2^{11}	4380	30,362
d91	2^{8}	2^{10}	7927	54,793
d92	2^{8}	2^{10}	7937	54,851
d93	2^{6}	2^{31}	1083	7497
d94	2^{7}	2^{10}	3607	24,973
d95	2^{8}	2^{11}	5408	37,414
d96	2^{9}	2^{10}	30,074	209,735
d97	2^{8}	2^{11}	21,311	148,543
d98	2^{8}	2^{11}	22,759	158,655
d99	2^{9}	2^{10}	59,140	412,804

Table 6: Family "e": List of unsatisfiable VLSAT-3 formulas written in QF_UFDT logic

name	card_{in}	card_{out}	#asserts	#ops
e00	56	16	1422	7438
e01	80	15	2984	15,205
e02	80	16	2985	15,253
e03	56	12	1418	7264
e04	164	11	13,018	65,233
e05	196	11	18,721	93,748
e06	70	14	1576	8125
e07	118	14	4890	24,695
e08	198	10	11,173	55,980
e09	39	14	451	2500
e10	57	13	1261	6513
e11	136	28	8683	44,493
e12	56	17	1423	7489
e13	124	13	5445	27,433
e14	203	14	13,126	65,875
e15	65	14	1435	7420
e16	231	11	17,648	88,383
e17	306	11	23,928	119,783
e18	34	15	382	2195
e19	56	13	1419	7303
e20	112	12	5963	29,989
e21	120	17	6871	34,729
e22	85	14	2005	10,270
e23	80	17	2986	15,304
e24	220	15	15,636	78,465
e25	259	11	16,530	82,793
e26	122	14	4662	23,555
e27	118	15	4891	24,740
e28	140	18	8627	43,558
e29	244	11	15,900	79,643
e30	70	17	1579	8269
e31	72	14	1948	9985
e32	161	11	6186	31,073
e33	196	12	18,722	93,784
e34	80	20	2989	15,475
e35	127	11	3885	19,568
e36	216	11	11,924	59,763
e37	310	11	23,771	118,998
e38	49	15	779	4180
e39	128	11	4067	20,478
e40	124	14	5446	27,475
e41	166	12	13,352	66,934
e42	48	13	718	3798
e43	156	11	7050	35,393
e44	168	20	8411	42,585
e45	140	19	8628	43,615
e46	37	13	422	2318
e47	39	15	451	2540
e48	45	13	646	3438
e49	79	19	1960	10,275

name	card_{in}	card_{out}	#asserts	#ops
e50	74	13	1844	9428
e51	141	11	5923	29,758
e52	169	11	7133	35,808
e53	201	17	12,460	62,674
e54	41	14	501	2750
e55	87	14	2598	13,235
e56	174	21	9097	46,073
e57	155	14	9186	46,175
e58	61	16	1202	6338
e59	129	12	3518	17,764
e60	113	19	3915	20,050
e61	129	11	4054	20,413
e62	100	11	2539	12,838
e63	118	11	2611	13,198
e64	124	11	2768	13,983
e65	135	11	3118	15,733
e66	140	12	7273	36,539
e67	132	12	8072	40,534
e68	182	11	8875	44,518
e69	268	13	25,434	127,378
e70	96	11	2523	12,758
e71	176	21	9332	47,248
e72	628	16	21,528	107,968
e73	236	11	23,476	117,523
e74	137	11	4890	24,593
e75	212	12	10,265	51,499
e76	145	13	4125	20,833
e77	166	12	10,260	51,474
e78	182	12	15,492	77,634
e79	228	12	25,445	127,399
e80	32	13	236	1388
e81	162	12	10,199	51,169
e82	222	11	21,186	106,073
e83	32	14	493	2710
e84	61	19	1735	9150
e85	65	12	1763	8989
e86	140	12	8621	43,279
e87	67	11	1545	7868
e88	245	13	11,808	59,248
e89	309	12	21,686	108,604
e90	220	14	23,406	117,275
e91	96	24	4273	22,145
e92	173	11	7665	38,468
e93	170	12	11,340	56,874
e94	241	12	13,389	67,119
e95	328	12	25,257	126,459
e96	546	11	138,321	691,748
e97	621	43	149,152	748,383
e98	202	12	16,260	81,474
e99	48	31	1065	6658

Table 7: Family "f": List of unsatisfiable VLSAT-3 formulas written in QF_UFIDL logic

name	card_{in}	card_{out}	#asserts	#ops
f00	∞	∞	1463	9406
f01	∞	∞	13,172	70,315
f02	∞	∞	18,871	112,070
f03	∞	∞	3050	18,949
f04	∞	∞	6975	39,718
f05	∞	∞	8750	50,200
f06	∞	∞	1463	9151
f07	∞	∞	3050	17,770
f08	∞	∞	6064	33,625
f09	∞	∞	1463	9529
f10	∞	∞	6975	40,033
f11	∞	∞	13,172	70,777
f12	∞	∞	8068	47,714
f13	∞	∞	8193	44,890
f14	∞	∞	9523	51,850
f15	∞	∞	1306	8403
f16	∞	∞	5449	31,000
f17	∞	∞	25,662	135,211
f18	∞	∞	1633	10,690
f19	∞	∞	8750	50,569
f20	∞	∞	13,507	72,514
f21	∞	∞	1133	7750
f22	∞	∞	1463	9649
f23	∞	∞	9251	56,237
f24	∞	∞	3050	19,135
f25	∞	∞	3460	21,283
f26	∞	∞	17,869	95,676
f27	∞	∞	5890	33,876
f28	∞	∞	10,953	59,310
f29	∞	∞	13,415	74,535
f30	∞	∞	476	3740
f31	∞	∞	1487	10,063
f32	∞	∞	22,639	123,370
f33	∞	∞	568	4325
f34	∞	∞	698	5151
f35	∞	∞	4974	28,765
f36	∞	∞	1287	9550
f37	∞	∞	1487	9913
f38	∞	∞	24,224	129,551
f39	∞	∞	1248	8546
f40	∞	∞	1633	11,185
f41	∞	∞	16,805	93,685
f42	∞	∞	599	4400
f43	∞	∞	1907	12,898
f44	∞	∞	2318	14,684
f45	∞	∞	918	6595
f46	∞	∞	2477	15,670
f47	∞	∞	16,183	88,597
f48	∞	∞	1113	7942
f49	∞	∞	3362	19,815

name	card_{in}	card_{out}	#asserts	#ops
f50	∞	∞	7816	43,871
f51	∞	∞	1140	8560
f52	∞	∞	1245	8468
f53	∞	∞	1642	10,313
f54	∞	∞	320	2400
f55	∞	∞	1778	11,856
f56	∞	∞	21,296	135,145
f57	∞	∞	716	4905
f58	∞	∞	2465	15,380
f59	∞	∞	2609	15,596
f60	∞	∞	1017	7738
f61	∞	∞	2473	15,700
f62	∞	∞	13,541	76,345
f63	∞	∞	2255	13,557
f64	∞	∞	3491	20,145
f65	∞	∞	17,209	92,203
f66	∞	∞	688	4787
f67	∞	∞	2029	12,948
f68	∞	∞	15,140	81,175
f69	∞	∞	1506	10,733
f70	∞	∞	3008	18,683
f71	∞	∞	17,483	93,947
f72	∞	∞	7828	43,847
f73	∞	∞	13,122	71,815
f74	∞	∞	18,528	101,246
f75	∞	∞	2783	17,557
f76	∞	∞	5350	31,205
f77	∞	∞	12,010	68,885
f78	∞	∞	1210	8552
f79	∞	∞	1227	8563
f80	∞	∞	8750	52,015
f81	∞	∞	756	5183
f82	∞	∞	45,060	234,207
f83	∞	∞	46,286	241,214
f84	∞	∞	9895	54,409
f85	∞	∞	36,971	194,630
f86	∞	∞	144,336	740,733
f87	∞	∞	51,099	267,146
f88	∞	∞	1080	7680
f89	∞	∞	1321	8410
f90	∞	∞	10,563	58,460
f91	∞	∞	11,111	61,498
f92	∞	∞	28,173	171,962
f93	∞	∞	31,647	167,323
f94	∞	∞	31,597	167,073
f95	∞	∞	36,045	212,498
f96	∞	∞	40,702	213,845
f97	∞	∞	54,201	282,712
f98	∞	∞	24,050	127,399
f99	∞	∞	25,412	136,444

Table 8: Family "g": List of satisfiable VLSAT-3 formulas written in QF_BV logic

name	#variables	card	#asserts	#ops
g00	127	2^{46}	7987	40,041
g01	238	2^{27}	9157	45,517
g02	160	2^{62}	12,490	62,618
g03	160	2^{63}	12,490	62,626
g04	224	2^{89}	15,832	79,416
g05	192	2^{93}	18,397	92,337
g06	200	2^{80}	19,735	98,907
g07	233	2^{52}	23,058	115,232
g08	310	2^{40}	24,071	120,047
g09	224	2^{84}	24,788	124,156
g10	273	2^{55}	29,938	149,576
g11	366	2^{41}	33,438	166,778
g12	277	2^{38}	34,144	170,462
g13	313	2^{52}	37,418	186,872
g14	313	2^{57}	37,418	186,912
g15	299	2^{52}	38,293	191,275
g16	353	2^{53}	45,498	227,200
g17	353	2^{54}	45,498	227,208
g18	353	2^{57}	45,498	227,232
g19	385	2^{39}	45,580	227,434
g20	321	2^{44}	46,286	231,132
g21	329	2^{49}	52,913	264,291
g22	451	2^{56}	59,422	296,648
g23	519	2^{53}	63,046	314,608
g24	455	2^{44}	85,677	427,819
g25	138	2^{69}	9282	46,678
g26	139	2^{61}	9428	47,342
g27	201	2^{79}	12,645	63,447
g28	202	2^{71}	15,452	77,416
g29	194	2^{53}	16,918	84,618
g30	210	2^{73}	17,096	85,636
g31	210	2^{74}	17,096	85,644
g32	305	2^{62}	18,569	92,723
g33	228	2^{76}	19,386	97,074
g34	248	2^{99}	19,689	98,733
g35	341	2^{65}	21,828	108,970
g36	233	2^{54}	23,058	115,248
g37	219	2^{69}	23,292	116,566
g38	252	2^{51}	31,379	156,791
g39	308	2^{106}	34,025	170,349
g40	315	2^{91}	43,690	218,540
g41	415	2^{48}	47,966	239,376
g42	415	2^{49}	47,966	239,384
g43	473	2^{50}	53,819	268,541
g44	365	2^{50}	60,276	301,042
g45	428	2^{44}	62,937	314,173
g46	159	2^{68}	11,229	56,363
g47	160	2^{60}	12,490	62,602
g48	290	2^{59}	16,805	83,909
g49	200	2^{77}	19,735	98,883

name	#variables	card	#asserts	#ops
g50	273	2^{52}	29,938	149,552
g51	299	2^{53}	38,293	191,283
g52	353	2^{52}	45,498	227,192
g53	459	2^{47}	49,154	245,220
g54	325	2^{66}	52,331	261,525
g55	120	2^{60}	7029	35,377
g56	157	2^{56}	12,212	61,186
g57	248	2^{98}	19,689	98,725
g58	320	2^{65}	20,421	101,977
g59	233	2^{32}	23,904	119,302
g60	273	2^{51}	29,938	149,544
g61	263	2^{32}	30,228	150,862
g62	313	2^{53}	37,418	186,880
g63	421	2^{43}	51,099	254,989
g64	459	2^{48}	63,423	316,573
g65	164	2^{100}	13,466	67,794
g66	216	2^{75}	22,500	112,660
g67	249	2^{86}	23,764	119,002
g68	224	2^{92}	15,832	79,440
g69	200	2^{101}	19,625	98,525
g70	441	2^{21}	25,411	126,333
g71	220	2^{56}	23,613	118,065
g72	374	2^{56}	40,702	203,202
g73	187	2^{79}	17,173	86,115
g74	228	2^{132}	25,662	128,902
g75	444	2^{47}	47,338	236,170
g76	549	2^{56}	70,640	352,542
g77	192	2^{91}	18,397	92,321
g78	400	2^{95}	74,565	372,777
g79	159	2^{104}	12,665	63,831
g80	308	2^{107}	34,025	170,357
g81	326	2^{65}	40,287	201,295
g82	315	2^{90}	43,690	218,532
g83	423	2^{50}	54,201	270,551
g84	309	2^{59}	17,964	89,666
g85	313	2^{51}	37,418	186,864
g86	216	2^{72}	22,500	112,636
g87	560	2^{59}	75,758	378,134
g88	194	2^{52}	16,918	84,610
g89	357	2^{38}	30,391	151,537
g90	248	2^{97}	19,689	98,717
g91	308	2^{109}	34,025	170,373
g92	410	2^{83}	83,441	417,041
g93	300	2^{150}	44,559	223,387
g94	250	2^{51}	30,881	154,305
g95	312	2^{108}	35,160	176,032
g96	176	2^{49}	13,719	68,627
g97	304	2^{72}	42,220	211,060
g98	412	2^{83}	84,259	421,127
g99	300	2^{100}	44,850	224,442

Table 9: Family "h": List of satisfiable VLSAT-3 formulas written in QF_DT logic

name	#variables	card	#asserts	#ops
h00	120	84	6938	27,784
h01	138	119	9497	42,531
h02	138	118	9496	42,292
h03	138	113	9491	41,127
h04	215	124	19,328	73,234
h05	200	129	19,553	75,169
h06	200	130	19,554	75,430
h07	194	193	18,869	93,661
h08	200	137	19,561	77,313
h09	200	139	19,563	77,869
h10	194	173	18,849	86,301
h11	628	210	21,722	109,054
h12	244	99	22,493	77,179
h13	155	53	9225	30,429
h14	214	80	16,048	54,462
h15	237	101	18,474	65,520
h16	175	35	12,096	37,476
h17	263	29	27,162	82,296
h18	231	37	18,499	56,827
h19	271	54	33,926	104,638
h20	231	36	17,472	53,674
h21	258	43	21,183	65,353
h22	189	66	10,287	35,149
h23	296	36	23,011	70,291
h24	259	32	16,551	50,643
h25	231	36	18,498	56,752
h26	157	46	10,815	34,513
h27	282	162	37,101	137,383
h28	245	50	11,845	37,983
h29	172	44	14,142	44,316
h30	180	36	12,786	39,616
h31	324	37	29,130	88,720
h32	154	56	11,129	36,465
h33	154	57	11,130	36,580
h34	260	259	33,463	167,209
h35	288	195	37,422	150,094
h36	266	114	23,530	83,470
h37	287	117	31,277	107,401
h38	385	53	45,247	138,495
h39	323	135	48,601	163,891
h40	201	79	12,522	43,726
h41	270	28	31,245	94,489
h42	143	52	9150	30,100
h43	265	29	23,504	71,322
h44	261	50	12,661	40,431
h45	323	129	48,595	162,295
h46	285	26	29,014	87,690
h47	292	229	41,987	178,171
h48	270	29	16,946	51,648
h49	621	110	149,219	459,645

name	#variables	card	#asserts	#ops
h50	279	29	17,595	53,595
h51	282	31	25,260	76,708
h52	244	32	15,921	48,753
h53	233	32	23,702	72,096
h54	172	44	14,208	44,514
h55	408	407	67,406	367,458
h56	248	101	19,541	68,721
h57	500	204	119,303	399,319
h58	258	30	21,170	64,378
h59	621	114	149,223	460,549
h60	233	32	23,648	71,934
h61	302	210	42,839	172,405
h62	258	31	21,171	64,441
h63	500	202	119,301	398,503
h64	258	40	21,180	65,098
h65	293	119	32,621	111,903
h66	138	69	9212	32,326
h67	316	243	49,213	206,443
h68	258	39	21,179	65,017
h69	258	41	21,181	65,181
h70	284	26	28,792	87,024
h71	500	207	119,306	400,558
h72	260	53	13,333	42,753
h73	500	210	119,309	401,815
h74	258	33	21,173	64,573
h75	283	57	32,424	100,462
h76	319	222	45,664	186,052
h77	408	124	57,697	188,341
h78	961	62	446,926	1,344,558
h79	961	72	446,936	1,345,918
h80	333	37	33,496	101,818
h81	500	228	119,327	409,735
h82	224	50	21,418	66,702
h83	500	226	119,325	408,823
h84	159	68	11,137	37,965
h85	500	227	119,326	409,278
h86	501	500	105,952	567,354
h87	500	225	119,324	408,370
h88	272	31	18,201	55,531
h89	467	466	55,858	384,262
h90	500	218	119,317	405,255
h91	500	251	119,350	420,798
h92	258	34	21,174	64,642
h93	500	237	119,336	413,938
h94	258	38	21,178	64,938
h95	500	238	119,337	414,415
h96	194	57	16,780	53,530
h97	258	36	21,176	64,786
h98	500	229	119,328	410,194
h99	500	233	119,332	412,050

Table 10: Family "i": List of satisfiable VLSAT-3 formulas written in QF_IDL logic

name	#variables	card	#asserts	#ops
i00	215	∞	19,420	62,056
i01	236	∞	19,484	61,252
i02	228	∞	19,386	86,806
i03	200	∞	19,625	88,973
i04	160	∞	12,490	53,526
i05	273	∞	29,938	115,552
i06	150	∞	11,175	46,073
i07	191	∞	12,636	43,778
i08	270	∞	17,901	87,865
i09	159	∞	11,229	50,753
i10	162	∞	13,122	59,128
i11	287	∞	31,448	141,088
i12	244	∞	19,020	62,316
i13	315	∞	47,970	197,438
i14	489	∞	55,884	214,100
i15	112	∞	6064	27,186
i16	144	∞	8176	30,886
i17	159	∞	12,665	60,353
i18	252	∞	31,379	117,289
i19	527	∞	87,908	324,356
i20	625	∞	96,444	381,918
i21	584	∞	84,282	324,604
i22	584	∞	84,282	335,912
i23	480	∞	92,070	290,398
i24	249	∞	23,764	106,808
i25	502	∞	60,716	232,602
i26	589	∞	83,903	320,961
i27	559	∞	77,529	301,095
i28	579	∞	78,666	300,896
i29	625	∞	96,444	384,100
i30	170	∞	12,010	48,068
i31	329	∞	52,913	188,627
i32	625	∞	96,444	383,010
i33	224	∞	24,788	105,022
i34	498	∞	124,202	619,126
i35	498	∞	124,202	619,384
i36	260	∞	33,465	161,933
i37	277	∞	34,144	122,076
i38	623	∞	95,106	375,406
i39	623	∞	95,106	376,498
i40	498	∞	124,202	621,104
i41	524	∞	137,318	677,740
i42	405	∞	76,926	378,694
i43	645	∞	102,997	408,127
i44	645	∞	102,997	411,499
i45	219	∞	23,292	94,798
i46	409	∞	76,114	271,068
i47	615	∞	94,241	368,339
i48	164	∞	13,466	63,296
i49	606	∞	183,500	908,240

name	#variables	card	#asserts	#ops
i50	704	∞	245,856	1,176,046
i51	802	∞	309,062	1,427,170
i52	800	∞	314,447	1,512,047
i53	252	∞	31,647	139,789
i54	511	∞	130,476	653,056
i55	834	∞	218,412	683,318
i56	813	∞	300,190	1,493,444
i57	926	∞	378,528	1,795,514
i58	224	∞	24,788	104,740
i59	499	∞	124,750	623,748
i60	606	∞	183,500	908,440
i61	444	∞	47,338	181,586
i62	813	∞	300,190	1,520,938
i63	800	∞	314,447	1,482,059
i64	252	∞	31,597	133,105
i65	756	∞	153,961	599,233
i66	736	∞	267,936	1,288,878
i67	752	∞	282,287	1,391,359
i68	859	∞	298,000	996,732
i69	709	∞	130,363	526,635
i70	622	∞	192,992	941,358
i71	762	∞	290,182	1,451,944
i72	830	∞	342,480	1,672,436
i73	919	∞	361,735	1,362,921
i74	498	∞	124,202	619,214
i75	500	∞	125,250	626,248
i76	520	∞	135,460	677,298
i77	830	∞	342,480	1,717,166
i78	511	∞	130,449	647,427
i79	830	∞	338,025	1,634,371
i80	756	∞	153,961	600,551
i81	802	∞	321,602	1,608,804
i82	818	∞	324,914	1,566,002
i83	250	∞	30,881	115,591
i84	752	∞	282,437	1,413,559
i85	216	∞	22,500	94,064
i86	834	∞	347,625	1,739,261
i87	798	∞	168,909	678,521
i88	549	∞	70,640	270,326
i89	575	∞	165,568	827,900
i90	365	∞	60,366	215,146
i91	1098	∞	303,971	981,191
i92	560	∞	75,758	289,930
i93	804	∞	293,357	1,210,883
i94	490	∞	120,295	601,473
i95	160	∞	12,490	53,328
i96	1081	∞	451,115	1,364,133
i97	1329	∞	509,080	1,540,508
i98	575	∞	164,438	751,882
i99	1324	∞	497,123	1,501,947

Table 11: Family "j": List of satisfiable VLSAT-3 formulas written in QF_UFBV logic

name	card_{in}	card_{out}	#asserts	#ops
j00	2^{6}	2^{30}	1000	6908
j01	2^{6}	2^{25}	1250	8648
j02	2^{6}	2^{30}	1280	8853
j03	2^{6}	2^{30}	1665	11,533
j04	2^{6}	2^{30}	1719	11,911
j05	2^{7}	2^{40}	4770	33,168
j06	2^{11}	2^{98}	6048	42,200
j07	2^{11}	2^{108}	7768	54,215
j08	2^{8}	2^{51}	8610	59,968
j09	2^{8}	2^{32}	12,394	86,226
j10	2^{8}	2^{38}	16,841	117,406
j11	2^{8}	2^{93}	18,397	128,387
j12	2^{8}	2^{50}	18,611	129,787
j13	2^{8}	2^{100}	18,675	130,323
j14	2^{8}	2^{75}	18,975	132,373
j15	2^{8}	2^{120}	19,495	136,013
j16	2^{8}	2^{75}	19,735	137,693
j17	2^{8}	2^{199}	19,900	139,099
j18	2^{9}	2^{68}	21,399	149,153
j19	2^{9}	2^{69}	21,399	149,155
j20	2^{9}	2^{70}	21,399	149,157
j21	2^{9}	2^{71}	21,399	149,159
j22	2^{9}	2^{64}	21,696	151,341
j23	2^{12}	2^{81}	24,788	173,004
j24	2^{9}	2^{21}	25,411	176,594
j25	2^{9}	2^{75}	31,017	216,349
j26	2^{9}	2^{157}	33,964	237,274
j27	2^{9}	2^{51}	38,293	267,254
j28	2^{9}	2^{65}	40,287	281,159
j29	2^{9}	2^{229}	43,029	300,579
j30	2^{9}	2^{231}	43,029	300,583
j31	2^{9}	2^{232}	43,029	300,585
j32	2^{9}	2^{233}	43,029	300,587
j33	2^{9}	2^{234}	43,029	300,589
j34	2^{9}	2^{235}	43,029	300,591
j35	2^{9}	2^{236}	43,029	300,593
j36	2^{9}	2^{237}	43,029	300,595
j37	2^{9}	2^{238}	43,029	300,597
j38	2^{9}	2^{239}	43,029	300,599
j39	2^{9}	2^{240}	43,029	300,601
j40	2^{9}	2^{241}	43,029	300,603
j41	2^{9}	2^{51}	43,522	303,797
j42	2^{9}	2^{90}	43,690	305,063
j43	2^{9}	2^{44}	46,286	323,125
j44	2^{9}	2^{210}	49,105	343,193
j45	2^{9}	2^{108}	50,382	351,916
j46	2^{9}	2^{158}	60,144	420,215
j47	2^{10}	2^{73}	62,937	439,419
j48	2^{10}	2^{74}	62,937	439,421
j49	2^{10}	2^{75}	62,937	439,423

name	card_{in}	card_{out}	#asserts	#ops
j50	2^{10}	2^{77}	62,937	439,427
j51	2^{10}	2^{78}	62,937	439,429
j52	2^{9}	2^{14}	73,016	509,698
j53	2^{9}	2^{56}	76,114	531,681
j54	2^{9}	2^{56}	76,216	532,395
j55	2^{10}	2^{61}	77,529	541,146
j56	2^{10}	2^{63}	82,118	573,207
j57	2^{10}	2^{62}	83,903	585,676
j58	2^{9}	2^{43}	85,677	598,458
j59	2^{10}	2^{62}	87,124	608,163
j60	2^{9}	2^{21}	93,051	650,074
j61	2^{9}	2^{57}	114,402	799,432
j62	2^{9}	2^{81}	114,402	799,480
j63	2^{9}	2^{82}	114,402	799,482
j64	2^{9}	2^{83}	114,402	799,484
j65	2^{9}	2^{84}	114,402	799,486
j66	2^{9}	2^{85}	114,402	799,488
j67	2^{7}	2^{33}	2178	15,112
j68	2^{7}	2^{37}	2738	19,016
j69	2^{7}	2^{40}	2970	20,628
j70	2^{11}	2^{88}	5458	38,065
j71	2^{8}	2^{41}	9962	69,388
j72	2^{8}	2^{104}	12,665	88,384
j73	2^{9}	2^{30}	21,399	149,077
j74	2^{8}	2^{56}	23,613	164,741
j75	2^{8}	2^{132}	25,662	179,212
j76	2^{9}	2^{72}	42,220	294,770
j77	2^{9}	2^{14}	75,529	527,289
j78	2^{10}	2^{68}	3548	24,715
j79	2^{7}	2^{45}	3924	27,286
j80	2^{7}	2^{48}	5848	40,694
j81	2^{8}	2^{100}	13,466	93,968
j82	2^{7}	2^{50}	2745	19,073
j83	2^{7}	2^{60}	7029	48,961
j84	2^{7}	2^{64}	7680	53,502
j85	2^{8}	2^{36}	17,668	123,053
j86	2^{8}	2^{36}	18,694	130,235
j87	2^{7}	2^{53}	2956	20,565
j88	2^{7}	2^{38}	3524	24,475
j89	2^{7}	2^{60}	7200	50,158
j90	2^{9}	2^{150}	44,559	311,311
j91	2^{8}	2^{72}	20,264	141,342
j92	2^{9}	2^{41}	32,521	226,344
j93	2^{8}	2^{60}	11,010	76,708
j94	2^{12}	2^{80}	24,788	173,002
j95	2^{10}	2^{44}	62,937	439,361
j96	2^{7}	2^{53}	4518	31,445
j97	2^{8}	2^{92}	18,397	128,385
j98	2^{8}	2^{50}	11,175	77,873
j99	2^{8}	2^{68}	11,229	78,260

Table 12: Family "k": List of satisfiable VLSAT-3 formulas written in QF_UFDT logic

name	card_{in}	card_{out}	#asserts	#ops
k00	138	137	9515	75,249
k01	138	118	9496	67,953
k02	138	115	9493	66,900
k03	164	125	13,132	88,660
k04	200	126	19,550	121,123
k05	200	127	19,551	121,504
k06	200	136	19,560	125,068
k07	200	137	19,561	125,479
k08	200	138	19,562	125,893
k09	258	48	21,188	109,228
k10	194	174	18,850	139,055
k11	233	93	20,295	114,123
k12	258	44	21,184	108,670
k13	213	41	8455	44,653
k14	155	54	9226	50,315
k15	244	32	15,921	81,029
k16	241	26	13,403	67,938
k17	266	112	23,528	136,064
k18	167	35	10,978	56,605
k19	154	57	11,130	60,324
k20	189	66	10,287	57,738
k21	258	43	21,183	108,538
k22	134	53	8528	46,668
k23	249	26	13,916	70,503
k24	187	65	10,000	56,110
k25	247	30	15,528	78,885
k26	259	32	16,588	84,364
k27	296	35	23,010	116,765
k28	194	68	10,870	61,048
k29	265	29	23,504	118,680
k30	157	46	10,815	57,088
k31	168	35	11,143	57,430
k32	154	56	11,129	60,153
k33	265	29	23,537	118,845
k34	203	78	13,190	74,803
k35	292	34	26,255	132,890
k36	180	36	12,786	65,748
k37	274	171	35,066	218,593
k38	208	83	13,289	76,488
k39	252	201	31,545	217,623
k40	259	32	16,438	83,614
k41	270	29	16,946	85,890
k42	282	31	25,260	127,633
k43	260	216	33,420	236,328
k44	621	88	149,197	757,293
k45	621	104	149,213	761,925
k46	288	197	37,424	244,644
k47	265	209	34,792	238,750
k48	282	192	37,131	240,279
k49	172	44	14,142	73,460

name	card_{in}	card_{out}	#asserts	#ops
k50	233	32	23,648	119,664
k51	185	38	16,693	85,498
k52	258	41	21,181	108,283
k53	400	399	79,897	636,890
k54	621	95	149,204	759,225
k55	621	112	149,221	764,529
k56	201	79	12,522	71,695
k57	292	225	41,798	284,140
k58	159	68	11,137	62,383
k59	245	47	11,165	58,974
k60	187	38	17,059	87,328
k61	258	30	21,170	107,095
k62	233	32	23,702	119,934
k63	302	213	42,842	281,518
k64	172	44	14,208	73,790
k65	292	39	21,479	109,540
k66	256	16	9280	46,728
k67	245	50	11,845	62,800
k68	258	35	21,175	107,590
k69	295	27	30,957	155,784
k70	258	31	21,171	107,188
k71	316	204	42,756	275,490
k72	316	243	49,213	333,788
k73	150	50	11,074	58,945
k74	279	29	17,595	89,135
k75	258	32	21,172	107,284
k76	258	40	21,180	108,160
k77	258	42	21,182	108,409
k78	365	364	65,923	527,085
k79	261	50	12,661	66,880
k80	308	125	33,841	192,205
k81	500	216	119,315	665,803
k82	500	220	119,319	668,425
k83	500	229	119,328	674,500
k84	500	223	119,322	670,423
k85	500	226	119,325	672,448
k86	500	218	119,317	667,108
k87	500	222	119,321	669,754
k88	315	314	49,630	394,945
k89	2317	7	67,403	337,064
k90	277	53	14,251	75,283
k91	500	225	119,324	671,770
k92	451	38	58,696	295,513
k93	500	241	119,340	682,978
k94	194	57	16,780	88,574
k95	435	17	83,685	418,799
k96	500	243	119,342	684,433
k97	500	249	119,348	688,870
k98	500	232	119,331	676,579
k99	500	242	119,341	683,704

Table 13: Family "l": List of satisfiable VLSAT-3 formulas written in QF_UFIDL logic

name	card_{in}	card_{out}	#asserts	#ops
l00	∞	∞	19,625	144,910
l01	∞	∞	19,625	145,189
l02	∞	∞	19,625	147,565
l03	∞	∞	19,625	153,889
l04	∞	∞	19,625	156,805
l05	∞	∞	19,625	157,978
l06	∞	∞	13,890	158,430
l07	∞	∞	21,173	132,481
l08	∞	∞	17,209	104,878
l09	∞	∞	19,420	166,325
l10	∞	∞	16,918	111,755
l11	∞	∞	45,580	273,055
l12	∞	∞	12,108	93,498
l13	∞	∞	25,512	150,310
l14	∞	∞	24,224	152,474
l15	∞	∞	47,966	297,573
l16	∞	∞	24,725	154,603
l17	∞	∞	45,580	272,023
l18	∞	∞	32,105	258,500
l19	∞	∞	47,966	299,760
l20	∞	∞	32,105	250,382
l21	∞	∞	32,105	261,830
l22	∞	∞	5689	42,992
l23	∞	∞	36,971	215,672
l24	∞	∞	16,443	103,568
l25	∞	∞	23,058	149,877
l26	∞	∞	24,071	155,403
l27	∞	∞	38,293	235,010
l28	∞	∞	9521	59,019
l29	∞	∞	18,687	118,766
l30	∞	∞	35,170	285,487
l31	∞	∞	47,966	296,475
l32	∞	∞	11,111	70,969
l33	∞	∞	35,170	288,262
l34	∞	∞	37,222	295,533
l35	∞	∞	37,222	301,869
l36	∞	∞	32,521	480,524
l37	∞	∞	57,982	417,135
l38	∞	∞	15,332	155,238
l39	∞	∞	22,683	143,005
l40	∞	∞	46,406	375,310
l41	∞	∞	57,982	417,990
l42	∞	∞	47,970	388,525
l43	∞	∞	65,043	668,252
l44	∞	∞	12,212	85,119
l45	∞	∞	43,834	363,240
l46	∞	∞	16,666	106,186
l47	∞	∞	125,692	1,006,204
l48	∞	∞	35,624	222,364
l49	∞	∞	47,338	295,161

name	card_{in}	card_{out}	#asserts	#ops
l50	∞	∞	35,153	217,390
l51	∞	∞	45,762	378,581
l52	∞	∞	21,733	138,493
l53	∞	∞	164,523	1,555,162
l54	∞	∞	38,293	235,745
l55	∞	∞	77,738	632,091
l56	∞	∞	46,406	379,702
l57	∞	∞	65,043	672,530
l58	∞	∞	18,443	115,570
l59	∞	∞	37,418	233,652
l60	∞	∞	63,936	511,060
l61	∞	∞	77,738	617,841
l62	∞	∞	36,990	230,767
l63	∞	∞	54,201	335,497
l64	∞	∞	63,423	381,370
l65	∞	∞	164,523	1,553,947
l66	∞	∞	22,141	621,577
l67	∞	∞	55,352	451,949
l68	∞	∞	9117	61,366
l69	∞	∞	96,444	623,123
l70	∞	∞	95,106	619,200
l71	∞	∞	26,548	167,332
l72	∞	∞	72,225	680,480
l73	∞	∞	24,071	154,593
l74	∞	∞	82,118	536,371
l75	∞	∞	7401	56,958
l76	∞	∞	12,931	81,843
l77	∞	∞	56,145	466,238
l78	∞	∞	69,298	573,873
l79	∞	∞	148,022	1,222,049
l80	∞	∞	54,241	446,019
l81	∞	∞	65,248	533,565
l82	∞	∞	105,954	906,016
l83	∞	∞	76,532	624,755
l84	∞	∞	70,279	583,885
l85	∞	∞	99,132	637,527
l86	∞	∞	60,423	495,192
l87	∞	∞	282,437	2,260,054
l88	∞	∞	60,627	512,697
l89	∞	∞	77,240	649,222
l90	∞	∞	102,997	667,458
l91	∞	∞	17,096	130,103
l92	∞	∞	64,039	615,010
l93	∞	∞	245,802	1,967,854
l94	∞	∞	15,446	90,617
l95	∞	∞	68,549	576,499
l96	∞	∞	183,500	1,468,046
l97	∞	∞	10,635	67,890
l98	∞	∞	321,602	2,572,404
l99	∞	∞	79,681	652,354

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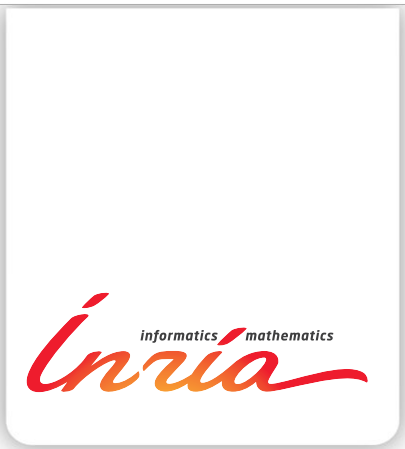

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