Robust FinFET Schmitt Trigger Designs for Low Power Applications

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Abstract. The IoT development alongside with the more pronounced impact of process variability in modern technology nodes, is the central reason to control variability impact. Given the broad set of IoT devices running on battery-oriented environments, energy consumption should be minimal and the operation reliable. Schmitt Trigger inverters are frequently used for noise immunity enhancement, and have been recently applied to mitigate radiation effects and variability impact. Yet, Schmitt Trigger operation at nominal voltage still introduces high deviation on power consumption. Thus, the main contribution of this work is to identify the relationship between transistor sizing, supply voltage, energy, and process variability robustness to achieve a minimal energy consumption circuit while keeping robustness. On average, scenarios with a lower supply voltage applied on layouts with a smaller number of fins, presented adequate robustness in high variability scenarios. Exploring voltage and transistor sizing made possible a reduction of about 24.84% on power consumption.

Keywords: Process Variability Mitigation · Schmitt Trigger · Low Power · FinFET technology

1 Introduction

Ultra-low Power (ULP) circuits are widely applied in various portable electronics applications such as cellular phones, bio-medical assistance devices and sensing networks. The ULP designs rise, alongside battery technology improvements, have provided us with portable, powerful and useful equipment for our daily routine, with wireless communication making information available anytime and anywhere [1][2]. One of the most proeminent ULP applicants is the Internet of Things (IoT) industry, determining technology development and industry tendencies.

As IoT devices emerged new kinds of applications have surfaced as well. From improving maintenance for all sorts of facilities, to sensor in remote areas and even automobile applications. However IoT applications still depend on an energy source, with battery-oriented applications being the most prominent. Given the limited life cycle of batteries, self-sufficient systems have appeared in order to alleviate the power consumption dilemma [2]. Given so, an IoT application will always be restricted by its power budget, with devices that can perform their functionality under heavy power constraints being essential [3]. The ideal circuit for ULP applications is the one that can perform a given task while consuming the least amount of energy. Such circuits might be achieved under transistor sizing and supply voltage tuning, being technology and application-dependent [2].

Nevertheless, the technology advance over transistor sizing has increased the density of chips and the challenges related to the manufacturing process, for example, the process variability and aging effects, the higher power consumption due to larger leakage currents, and the increase in the radiation-induced soft errors [4]. Multigate devices, as the Fin Field Effect Transistor (FinFET), have been proposed to help overcome some of those issues. The structure of FinFETs shows superior channel control due to the reduced short-channel effects (SCE) and diminished Random Dopant Fluctuation (RDF) effect due to the fully depleted channel [5]. However, process variability is one of the major challenges in nanometer technology, even on FinFET designs [6]. At deep nanotechnology nodes, each chip may show a distinct behavior due to process variations during the lithography steps in the manufacturing process. These variations exert influence over the metrics of the circuits such as performance and power consumption, which can bring unpredictable circuit degradation, making them unsuitable from its expected operation regime [4][7].

This work aims to explore a low power solution considering the effects of process variability in the Schmitt Trigger (ST) designs. ST circuits are widely applied on low power applications due to its noise immunity, and, recently have been considered for process variability mitigation on nanometer technologies. This set of data can provide relevant information for ULP designers, and also for other low power applications that need to manage process variability impact. Thus, the main contribution of this work is an in-depth evaluation of the influence of different factors on the ST design, considering: 1) multiple combinations of supply voltages; 2) different levels of process variability; and 3) the variable transistor sizing relation (number of fins). The experiments analysis the impact of these factors on the maximum achievable frequency within a failure threshold, the trade-off among these parameters and power consumption.

Next section aims to give more context to this work, commenting on related works and the main differences and contributions of this work in comparison. Section III gives a more in-depth explanation about variability and its several factors and phenomena. Section IV introduces the FinFET technology and the variability influence over it. Section V the main aspects of ST are shown as well its robustness enhancing capabilities. The methodology adopted to allow all the

evaluations is explained in Section VI. The results are discussed in Section VII and finally, Section VIII presents the main conclusions.

2 Related Work

Many works evaluate the effects of Process, Voltage and Temperature (PVT) variability on circuits and devices, but few works consider the effects for ULP designs.

Some works address theses issues focusing on the yield improvement. In [4] is developed a mathematical methodology for increase the yield considering aging, and PVT variability. With such method, the circuit sizing was optimized and, obeying some performance and power constraints, it was possible to achieve an increase from about 40% to 99% yield. [8] provides a characterization of the effects of open defects on nanoscale CMOS gates and circuits. It shows the difference on output value for several circuits, technology nodes and most important under the influence of PVT variability. In [9] is shown the implication of PVT variations on subthreshold device and circuit performance metrics. It was found that a $\pm 10\%$ on several transistor parameters could introduce up to a 77% variation in Energy, or Power-Delay Product (PDP). In this context, the use of STs is being investigated as an effective method for increasing the on-to-off current ratio, and consequently, for mitigating the process variation effects [3] on subthreshold operating systems.

Other works have evaluating the impact on arithmetic circuits, mainly on Full-Adders (FA). In [10] the effects of PVT variability in different Full Adder (FA) designs are investigated. Both Transmission Gate Adder (TGA) and Transmission Function Adder (TFA) architectures showed acceptable behavior under PVT variability with the lowest power consumption sensibility amongst the tested FAs, reaching about 11x smaller in comparison with Complementary Pass Transistor Logic (CPL) FA. In [11] simulations were performed on several FA circuits considering Carbon Nanotube Field Effect Transistor (CNFET) and bulk Complementary Metal-Oxide-Semiconductor (CMOS) technology. Results show that the TGA is the most robust circuit with its CNFET version providing up to 3x less variations. [12] presents a study about the delay variability caused by supply variations in the TGA. The experiments were performed at layout level. It showed that lower supply voltages bring more delay variability to the circuit with the TGA presenting worse results in comparison to static logic.

Given the energy constraints of ULP applications and the variability impact on recent nodes, the ST circuit has been pointed as an circuit-level alternative. The classical ST has been employed as a key element for several ULP circuits [13–16] and for variability mitigation, mainly attenuating the deviation on the power consumption. Schmitt Trigger was applied replacing internal inverters of full adders in [17], where spreads in major metrics were successfully limited. Also, the same experiment was executed at electrical and layout levels considering FinFET technology, and showed a considerable decrease in overall variability

impact on metrics [18][19]. However, with a considerable increase in delay and power consumption.

It is important to highlight that the mentioned works do not consider analysis at the layout-level in modern technology nodes. Additionally, most works do not consider such a combination of variables and even if they do, the analysis is often performed considering the circuit under the influence of only one of the variables at a time. This work presents a layout-level analysis, considering all parasitics and electrical behavior related to transistor placement and routing, as well as all considered variables exerting their influence at the same time, as would occur on a real scenario.

3 On Variability

As technology scaling advanced, decreasing the transistor dimensions, the ratio between device geometrical parameters and the atom-size itself have been shrinking. Multiple techniques have been developed to reduce the loss of precision due to the manufacturing process at different end-of-lines. However, as the quantum-mechanical limit approaches, manufacturing-induced imprecision impact rises [20].

Variability consists of characteristic deviations, internal or external to the circuit, which can determine its operational features and can be divided by three types concerning its sources: Environmental Factors - External factors to the circuits e.g. temperature and supply voltage variations [7, 21], Reliability Factors - related to the aging process e.g. Negative Bias Temperature Instability (NBTI), electromigration, dielectric breakdown and Hot Carrier Injection (HCI) [22–25, 7, 21] and Physical Factors - caused by the manufacturing process, consequence of imprecision in the manufacturing process which can be systematic, design dependent or random [21, 26–32]. Fig. 1, depicts the transistor intrinsic variability.

Despite the multiple advantages of new technologies, the atom scale makes process variability one of the most relevant challenge. FinFET devices have been investigated about the variability impact and the next subsection introduces the main concepts about FinFET technology to understand the variability impact on this device.

3.1 FinFET Technology and Variability Impact

The FinFET main geometric parameters are the gate length (L or L_G), fin width (W_{FIN}, T_{FIN} or T_{SI}), fin height (H_{FIN}) and Oxide Thickness (T_{OX}). FinFET transistors can be built on a traditional bulk or on a Silicon on Insulator (SOI) substrate with a conducting channel that rises above the level of the insulator, creating a thin silicon structure, the gate, as shown in Fig. 2 and Fig. 3.

The channel being surrounded from three dimensions by the gate results in a superior control, reduced SCE and RDF effect due to the fully depleted channel that causes less sensitivity to process variations [34]. FinFETs also present

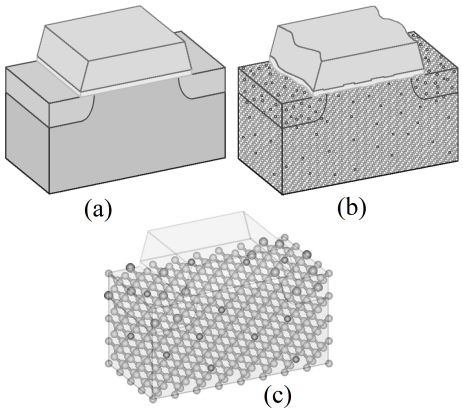

Fig. 1. Levels of abstraction from a ideal transistor towards a realistic concept. (a) Depicts a the current approach of semiconductor device simulation. (b) Depicts a 20-nm Metal-Oxide-Semiconductor FET (MOSFET). (c) Depicts a 4-nm MOSFET. [28].

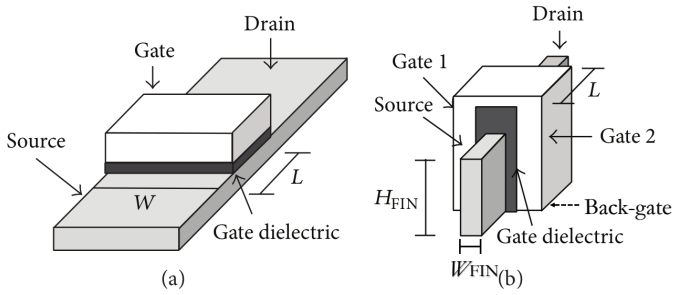

Fig. 2. Structural comparison between (a) planar MOSFET and (b) FinFET transistors. Modified from [33].

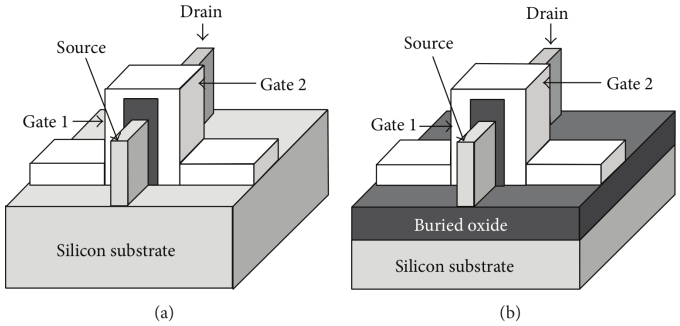

Fig. 3. Structural comparison between (a) bulk and (b) SOI FinFETs [33].

relative immunity to gate Line Edge Roughness (LER), a major source of variability in planar nanoscale FETs [35]. Overall, the major sources of variability expected for FinFETs are the L_G, W_{FIN}, H_{FIN} and gate WF [36]. Amongst all variability sources, it is shown that the V_t is mainly set by the gate WF, with fluctuations having a direct impact on its limits [37–40].

Given the challenges intrinsic to the adoption of high-k dielectrics in order tackle the increasing gate leakage due to the scaling down of gate oxide, a metal gate was adopted on FinFET devices [41–44]. Metals exist *in natura* in the form of crystals where each atom has several bonds with adjacent atoms. Although, due to defects and disorientation, several crystals are formed, with "grain boundaries" between regions of regularity (crystal grains) in the metal [45].

The electrostatic potential (e.g. V_t) varies depending on each grain boundary, as shown in Fig. 4. At Table 1 a example of possible orientation, probability and WF is given. Between several technology nodes - FD-SOI, Bulk and FinFET - the latter showed the lowest V_t variation due to the much larger gate area [45].

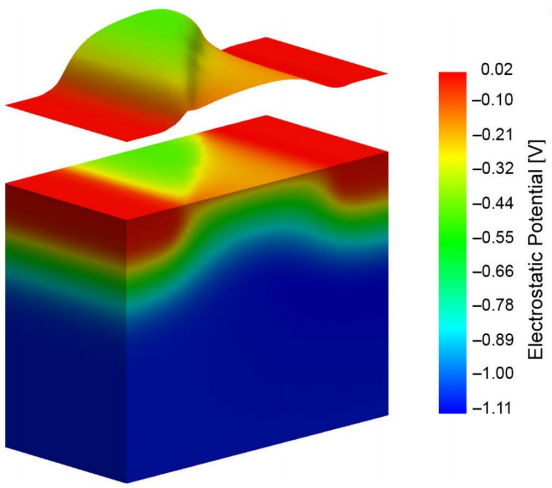

Fig. 4. Electrostatic potential in a generic 30-nm MOSFET with the surface potential shown below. The metal gate has two grains with the grain boundary diagonally across the channel [46].

Table 1. Metal orientation, probability and related work function [46].

Orientation	Probability	Work Function
<200>	60%	4.6 eV
<111>	40%	4.4 eV

The main source of variability on FinFETs arises from the metal gate granularity (MGG) that provokes significant work-function fluctuations (WFF), affecting the threshold voltage and the I_{on}/I_{off} currents [6][47].

4 Schmitt Trigger for Process Variability Mitigation

Schmitt Trigger circuits present a hysteresis characteristic. Hysteresis exists in the presence of two switching threshold voltages (V_t). If the input level is inside the hysteresis interval, the ST will not switch. Such characteristic provides a higher static noise margin (SNM) in comparison to traditional inverters, ensuring a high noise immunity. Deviations in physical parameters became alarming at ultra-deep sub-micron (UDSM) nodes due to the following supply voltage scaling, making the circuits more susceptible to noise and electromagnetic interference due to the deterioration in SNM [48].

There are several ST topologies proposed in the literature. In [49], three threshold adjustable ST circuits are presented, wher two are semi-adjustable (only one threshold level can be adjusted) and one are a fully adjustable (both threshold levels can be adjusted) topology. All circuits presents small chip area, and very low static power consumption. A higher performance ST is proposed in [50] where, by a different design, a smaller load capacitor value is achieved, decreasing the slew rate of the ST internal node.

In [51] a low-power ST is proposed as well by forward body biasing, decreasing the V_t, improving performance and decreasing the short circuit current. [52] proposes a 10T ST which its hysteresis interval does not depend on transistors width/length ratios being, consequently, more robust to process variations.

In [53] a ST with a programmable hysteresis is proposed. The programmable hysteresis is achieved by adding a P and N transistors in series with the 6T ST P_F and N_F transistors, respectively, both receiving the same gate signal. A low-power ST is proposed at [54] with low short circuit current achieved by the presence of only one path to each power rail, being recommended for low power, very low frequency applications. Additionally, [55] proposes a low-power ST by having only one transistor transmitting (at stable output values), considerably reducing power consumption.

As show in Fig. 5, this work explores a traditional ST topology, where the major difference from the most popular versions is the presence of P_F and N_F transistors [56]. These transistors are responsible for a feedback system. For example, if the output is at a high level, the N_F is closed, pulling the node X to a high potential, and forcing the drain-source voltage of transistor N_I almost zero and its gate-source voltage into the negative region. This kind of arrangement reduces the leakage current N_I exponentially, increasing the I_{on}/I_{off} current ratio, minimizing the output degradation [16].

The main effect of process variability on ST circuits is a shift in the Voltage Transfer Curve (VTC) due to the threshold voltage variation. Mostly, the input voltage, where a device starts transmitting current, is directly dependent on the V_t. Given so, the variability impact onto the VTC is reduced as a result of the

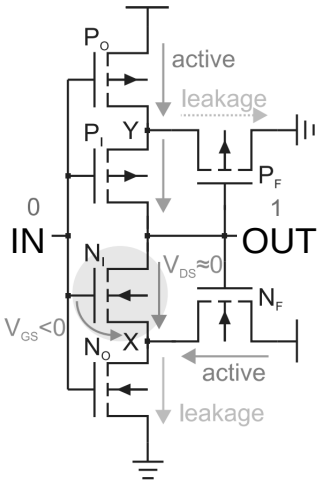

Fig. 5. ST inverter leakage suppression [16].

high influence of the gate-source voltage of the ST inner transistors (N_I and P_I) over its switching point [16].

5 Methodology

To present an broad exploration of power consumption and the process variability effects on the ST characteristics, this work evaluates: 1) ST circuit operating at multiple combinations of supply voltages; 2) the impact of different levels of process variability; 3) the influence of the transistor sizing exploring devices with different number of fins, all at the same time composing over 175 possible scenarios. The impact of these parameters on the maximum achievable frequency within a failure threshold will be analysed.

The design flow is shown at Figure 6. The project was divided into two main steps: the layouts designing and electrical simulations. After finishing the layout design process, each layout passed through validation which consisted of a Design Rule Checking (DRC) to detect if the layout obeys the technology geometry restrictions and layer rules, Layout Versus Schematic (LVS) where layout and schematic are compared to detect their equivalence (same nodes and nets) and a Behavioral test, in order to observe if the circuit works as expected at nominal operation.

5.1 Layout Design

All ST layouts were designed on the Virtuoso tool from Cadence® with the process design kit (PDK) of 7-nm FinFET (ASAP7) from the Arizona State University in partnership with ARM [57]. This PDK was chosen due to a realistic design conjecture regarding the current design competencies and for being

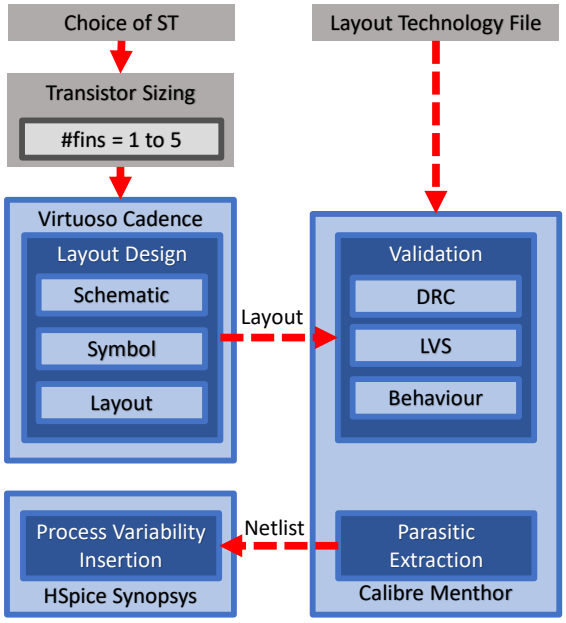

Fig. 6. Design flow of the experiments.

available for academic use. FinFET technologies present the width quantization aspect [58]. With a 27nm fin pitch, a high-density layout is achieved with 3-fins transistors. Otherwise, for a higher fin count, there is a lower density and routing complexity [59]. The main PDK rules and lithography assumptions considered in this work are shown in Table 2. The main layers and the 3-fin ST are shown in Fig. 7.

Table 2. Key layer lithography assumptions, widths and pitches [57].

Layer	Lithography	Width/drawn (nm)	Pitch (nm)
Fin	SAQP	6.5/7	27
Active (horizontal)	EUV	54/16	108
Gate	SADP	21/20	54
SDT/LISD	EUV	25/24	54
LIG	EUV	16/16	54
VIA0-VIA3	EUV	18/18	25
M1-M3	EUV	18/18	36

This work evaluates the ST with 1 to 5 fins. For comparison, the 1 and 5-fins layouts are shown in Fig. 8. For the layouts with 1 and 2 fins, due to the minimum active area technology restriction, it was not possible to lower the cell area in comparison to the 3-fins layout. Although considering a possible scenario, the

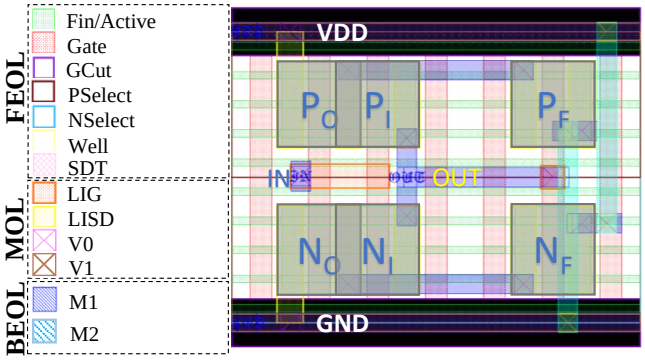

Fig. 7. 3-fins variant ST layout in 7nm FinFET Technology (ASAP7) [60]

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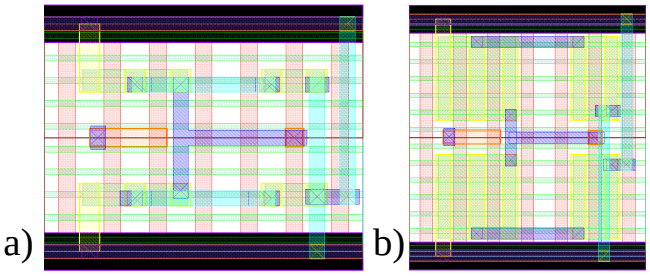

Fig. 8. a) 1 and (b) 5-fins ST layouts

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2 and 1-fin layouts would present a 20% and 40% reduction in area, compared to the 3-fins variant, respectively. The 3, 4 and 5-fins ST area, height and area increase are shown at Table 3.

It is important to clarify that a lower fin count does not necessarily mean an area reduction. The routability could turn into a challenge and a width of height increase would be necessary.

The ASAP7 PDK contains the manufacturing process composed by front end of line (FEOL), middle of line (MOL) and back end of line (BEOL). The layouts were developed in a continuous diffusion layer with every gate surrounding another gate in the horizontal axis. The Source-Drain Trench (SDT) connects the active area to the LISD layer. The Local-Interconnect Gate (LIG) is applied to connect the gate terminal, and Local-Interconnect Source-Drain (LISD) is used to connect the source and drain of the transistors. The function of V0 is to join the LIG and LISD to the BEOL layers. The Metal 1 (M1) is used for intra-cell routing and short connections. The Metal 2 (M2) was applied to connect the P_F and N_F drains to ground and source, respectively. For the layouts with a fin count below 3, M2 was applied to connect the source/drain of the P_F and

Table 3. 3, 4 and 5-fins STs area, height (in tracks of Metal 2), and the area increase corresponding to each extra fin.

#Fins	Area (nm^2)	Height (M2 Tracks)	Area increase
3	131220	7.5	-
4	157464	9	20%
5	183708	10.5	40%

N_F transistors to the X and Y layout nodes. Given the smaller area to work with, it was necessary to apply M2 in order to respect the M1 spacing rules, bringing to light one of the challenges related to a smaller layout. The M2 usage in those cases will increase the design parasitics from the neccessary extra vias connecting M1 and M2. To successfully pass the LVS step, it was necessary the addition of a TAP-cell to connect the transistors back-gates.

5.2 Electrical Simulation

The simulations were carried out in HSPICE [61] using the netlist obtained after the physical verification flow and the parasitic extraction. The reference values from ASAP7 technology for electrical simulations are shown in Table 4. For a more realistic test-bench, it was considered a scenario where the ST receives the signal from two inverters and drives a 1fF output capacitance, as shown in Fig. 9. The same supply voltage is applied in the entire testbench. Only the ST suffers from variability, and the inverters are the same (3-fins transistors) for all experiments. All designs present in the test-bench, inverters and ST, are simulated from the extracted layouts.

Table 4. Parameters applied in the electrical simulations [57].

Parameter	**7nm**	
Nominal Supply Voltage	0.7 V	
Gate Length (Lg)	21nm	
Fin Width (Wfin)	6.5nm	
Fin Height (Hfin)	32nm	
Oxide Thickness (Tox)	2.1nm	
Channel Doping	$1x10^{22}m^{-3}$	
Source/Drain Doping	$2x10^{22}m^{-3}$	
Work Function	NFET	4.372 eV
	PFET	4.8108 eV

The process variability evaluation was taken through 2000 Monte Carlo (MC) simulations [58] varying the WF of devices according to a Gaussian distribution considering a 3σ deviation. This work explores the behavior of ST with variations from 1% up to 5%. For each step on WF variation, all simulations were carried

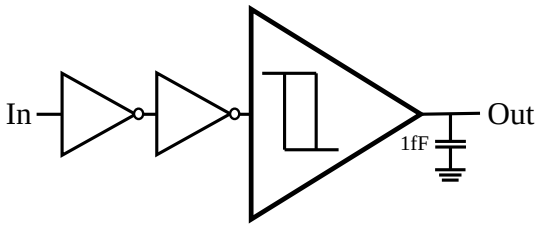

Fig. 9. Test-bench applied in all simulations [60].

from 0.1V to 0.7V supply voltage, with steps of 0.1V at a nominal temperature of 27°C. The voltage of 0.1V shows to be the technological limit to work without the loss of the hysteresis characteristic. For all experiments, it was observed maximum values, mean (μ), standard deviation (σ) and normalized standard deviation (σ/μ) for each metric: hysteresis interval, delay, and energy, where σ/μ represents the sensibility of the cell to process variability.

Due to the variability impact a circuit may present performance degradation, given that, in order to determine the maximum frequencies for the layouts evaluated, this work considers a 10% maximum failure threshold in the Monte Carlo simulations. Failures are defined as cases where a pair of operations (high-to-low and low-to-high) propagation times do not fit into the determined frequency. In the case of a number of failures above 10%, the frequency is decreased.

6 Results and Discussion

This section is divided into three parts. First, a discussion concerning energy consumption where a scenario-specific analysis is performed, and different sets of fin count and supply voltage are recommended. A performance analysis (delays and maximum frequencies) will follow, presenting an analysis of the fin count and supply voltage over absolute and deviation values. And finally, the ST hysteresis interval values are presented in relation to the variability level and number of fins.

6.1 Energy Consumption

For each level of WFF explored in this work, there is a distinct ideal scenario for each kind of application. As shown in Table 5, considering the absolute energy consumption observed, the 1-fin layout showed, in all cases, the lowest. It is due to its smaller driving capability, resulting in smaller currents.

The supply voltage recommended for each scenario increases almost linearly in relation to the level of WFF variability. The 0.1V regime did not prevail as the best option across all scenarios, shows the dependency of energy consumption with propagation times. Fig. 10 shows an average between the each particular variability scenario related to the number of fins. It can be observed a difference

Table 5. Recommended setup by each specific scenario [60].

WFF	Lowest Energy		Most Robust		Cost-Benefit	
	# Fins	Supply (V)	# Fins	Supply (V)	# Fins	Supply (V)
1%	1	0.1	1	0.7	1	0.7
2%	1	0.2	1	0.7	1	0.7-0.2
3%	1	0.2	5	0.3	1	0.3
4%	1	0.3	5	0.4	1	0.4
5%	1	0.4	5	0.5	1	0.5

above 100%, between maximum and minimum, showing a higher dependence of the number of fins in determining the circuits energy consumption. Results below 0.3V did not feature the chart in order to preserve its scale, since for 0.2V and 0.1V there are a 1 and 2 orders of magnitude increase on energy consumption, respectively.

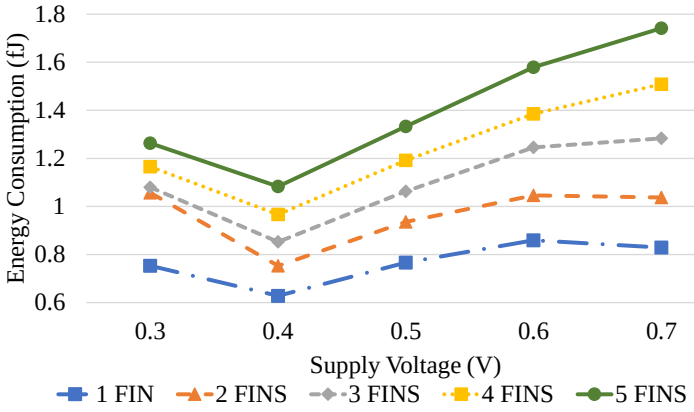

Fig. 10. Average energy consumption over supply voltage scaling [60].

Into the robustness analysis, a shift can be observed. For lower variability scenarios the setup recommended is at 1 fin layout and 0.7V for 1% and 2% WFF. From moderate to high variability (3% to 5%), the 5 fins layout gains advantage with the supply voltage scaling linearly.

The energy robustness is mainly determined by variations in the I_{on} and, consequently, the time necessary for the circuit charging/discharging. At nominal supply voltages, the I_{on} falls into the saturation region with an exponential dependence over the V_t. Given that, variations on the V_t will result in exponential variations. With the supply voltage decrease, the I_{on} falls into the linear region, diminishing the impact of V_t variations on the I_{on}.

Thus, at low variability scenarios, close-to-nominal supply voltages will not suffer from the exponential V_t dependence, weakening its effect with high current

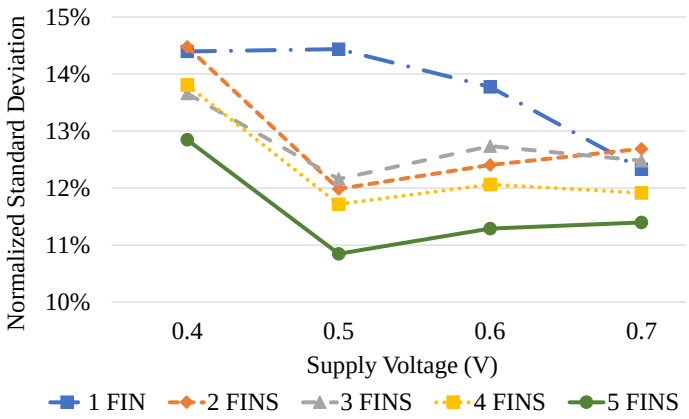

Fig. 11. Average energy consumption sensibility scaling over supply voltage [60].

peaks, small signal slopes overcharging and discharging and higher noise immunity. As variability rises, the linearity from the V_t will present an advantage, favoring smaller supply voltages. However, as variability rises again, the rise and variation in propagation times will start to determine the adequate supply voltage. Fig. 11, shows the average scaling on the impact of process variability on energy consumption. It can be seen a lower than 5% discrepancy between best and worst cases, showing the minor dependence of the number of fins in determining the circuits robustness. Results below 0.4V did not appear on the chart in order to preserve its scale. For 0.3V, 0.2V and 0.1V, maximum normalized standard deviations are 108.64%, 266.82% and 358%, respectively.

For the sake of comparison, Fig. 12 and Fig. 13 present the difference between the respective layouts with the lowest energy consumption and energy consumption variation and the traditional 3-fins layout. The highest difference was 27.85% and 14.44% for energy consumption and variability, respectively.

Considering a cost-benefit scenario, the best choice was defined by the lowest value given by the product of the energy consumption and the normalized deviation product (Energy-Deviation Product - EDP). It can be noticed a shift from a more robust layout (at 1% and 2% WFF) to a low energy layout at higher WFFs (3% to 5%). At 2% there are two supply voltages recommended since the EDP values similar. At this variability point the layout at 0.7V presents the highest robustness and acceptable energy consumption, due to the lower propagation times, while the layout operating at 0.2V presents the lowest energy consumption and acceptable energy deviation.

A comparison between the layouts with the lowest energy consumption, energy variability, and the best cost-benefit are shown in Figs. 14 and 15 in relation to energy consumption and energy variability, respectively. The energy variability of the lowest energy layout at 3% WFF is one example of why a cost-benefit analysis should be made since it shows an 11.5% lower energy consumption with a 582.47% higher sensibility.

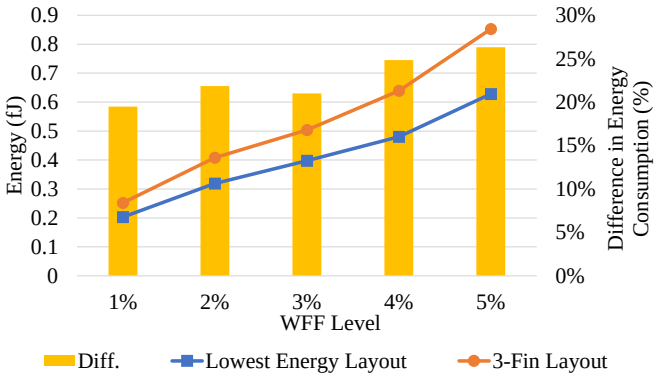

Fig. 12. Energy consumption comparison between the layout with the lowest energy consumption and the traditional 3-fins layout at the same supply voltage [60].

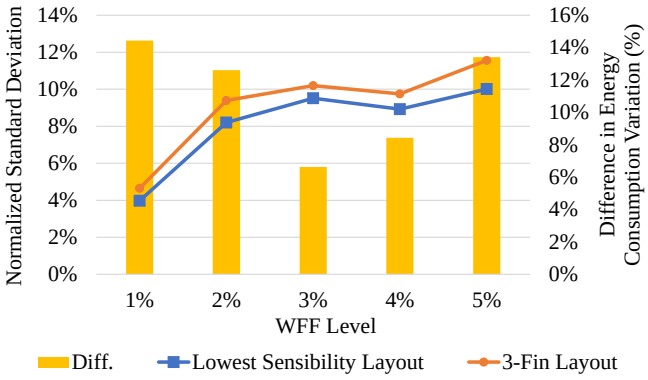

Fig. 13. Energy variability comparison between the layout with the lowest sensibility and the traditional 3-fins layout at the same supply voltage [60].

6.2 Propagation Delays and Maximum Frequencies

At performance scaling it can be observed a worsening on propagation times over the lowering of the supply voltage and fin count. The transistor driving capability is proportional to the fin count, given that with more fins there is a larger active area passing current, fastening the charging/discharging process. Given the area penalty, which will be discussed, the 4-fins layout only gives a 10% penalty on propagation times, being a good choice over area constraints in comparison to the 5-fins layout. The 3, 2 and 1 fins layouts bring a 42%, 92% and 268% delay increase on average, respectively.

In comparison to the traditional 3-fins layout, the 5 and 4-fins variants bring 20% and 13.612% decrease on propagation times while the 2-fins and 1-fin variants bring 27.24% and 107% delay increase, respectively.

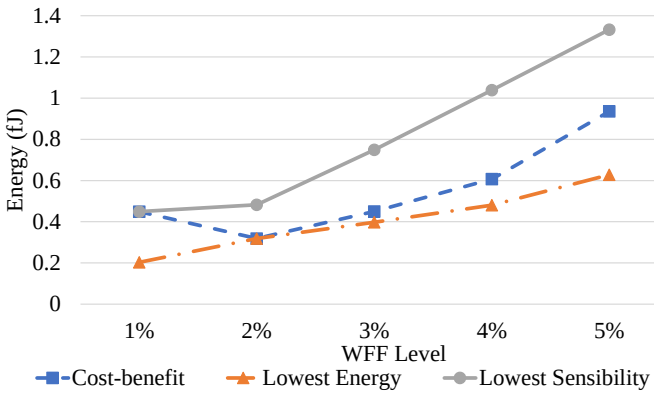

Fig. 14. Energy consumption comparison among the layouts with the best cost-benefit, lowest energy consumption and lowest variability sensibility [60].

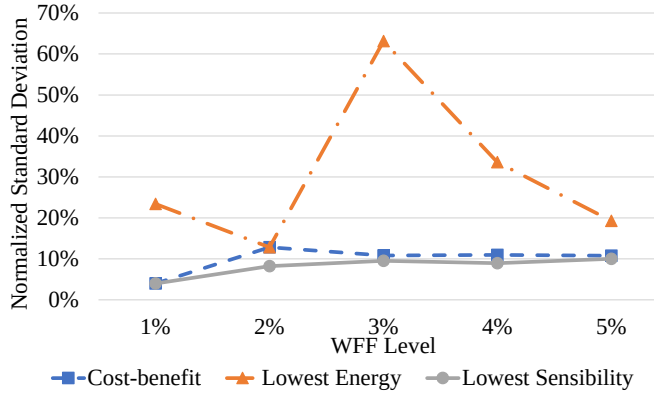

Fig. 15. Energy variability comparison among the layouts with the best cost-benefit, lowest energy consumption and lowest variability sensibility [60].

For variability impact, it can be observed a tendency of lower sensibility over higher fin count at higher supply voltages. As supply voltage scales down, a lower number of fins starts to keep up with the variability robustness, as shown in Fig. 16. It can be concluded that due to the exponential relation of drain current with gate-to-source voltage, the higher fin count is capable of providing the necessary current drive at higher supply voltages. At lower supply voltages, with the drain current decreasing exponentially, the fin count impact on variability robustness is diminished.

Maximum frequencies are shown at Table 6. The maximum frequencies are proportional to the supply voltage and fin count. The higher fin count allows faster charging and discharging due to a bigger active area driving current. On average, the 5 and 4-fins layouts were able to present 16% and 10.34% higher

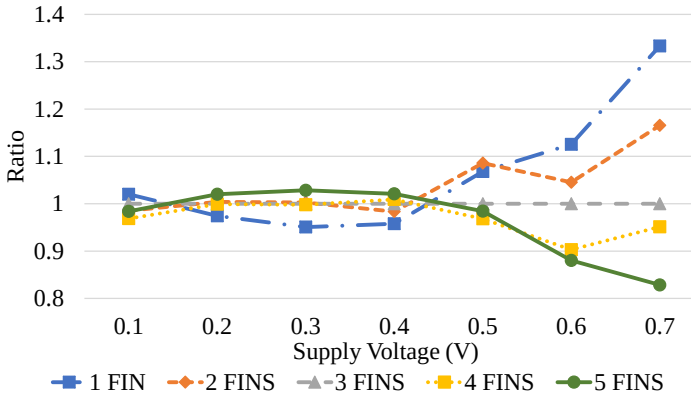

Fig. 16. Delay sensibility ratio between layouts [60].

frequencies while the 2 and 1-fin variants showed 19.18% and 44.65% lower frequencies, in comparison to the 3-fins variant.

Fig. 17 and Fig. 18 show the average ratio between the different variability and circuits scenarios normalized in relation to the 1 Fin layout and 5% WFF scenario, respectively. It can be noticed a considerable 52.597 times ratio between low and high variability scenarios, being the main variable determining the circuit frequency. In comparison, the number of fins brings a maximum 3.917 times ratio between 5 and 1 fins layouts, exposing the advantage of a higher number of fins on low supply voltages.

6.3 Hysteresis Interval

Hysteresis is one of the major characteristics related to the circuit ability to filter noise. A higher hysteresis interval brings more robustness to the circuit. As a priority, the ratio between its value and the supply voltage should be as high as possible. The ST, at nominal operation (nominal supply voltage and no process variability), presented a maximum hysteresis interval of approximately 0.45V. Given that, considering the average absolute values of the hysteresis interval, it can be observed a difference below than 5% between the best and worst cases, considering different fin counts.

At higher supply voltages of 0.6V and 0.7V, the difference widens up reaching up to 10.76% and 25.26% between the 5-fins and 1-fin layout, respectively. Such results come from the faster charging/discharging, which decreases the signal slopes widening the circuit hysteresis interval. At lower supply voltages, a decreased number of fins is sufficient to keep the slopes low enough, presenting high hysteresis to supply voltage ratios while at higher supply voltages a lower number of fins will increase the signal slopes.

Although, there is a hysteresis interval improvement, as shown in Fig. 19, over the WFF increase as well. Such behavior happens due to the hysteresis

Table 6. Each scenario respective maximum frequency.

WFF	# Fins	Supply Voltage (V)						
		0.1	0.2	0.3	0.4	0.5	0.6	0.7
1%	1	600KHz	15MHz	350MHz	2GHz	8GHz	12GHz	16GHz
	2	1.1MHz	25MHz	600MHz	4GHz	13GHz	19GHz	24GHz
	3	1.5MHz	35MHz	900MHz	5GHz	17GHz	24GHz	29GHz
	4	1.75MHz	40MHz	1GHz	6GHz	19GHz	27GHz	33GHz
	5	2.25MHz	50MHz	1.2GHz	6GHz	21GHz	30GHz	35GHz
2%	1	200KHz	5MHz	150MHz	1.5GHz	5GHz	11GHz	15GHz
	2	400KHz	9MHz	250MHz	2.5GHz	7GHz	18GHz	23GHz
	3	600KHz	12.5MHz	300MHz	3GHz	9GHz	22.5GHz	28GHz
	4	700KHz	15MHz	450MHz	4GHz	11GHz	17GHz	31GHz
	5	900KHz	18MHz	500MHz	4GHz	12GHz	20GHz	25GHz
3%	1	100KHz	2MHz	60MHz	1GHz	4GHz	8GHz	14GHz
	2	200KHz	3MHz	100MHz	1.5GHz	6GHz	11GHz	20GHz
	3	200KHz	5MHz	125MHz	2GHz	8GHz	14GHz	19GHz
	4	300KHz	6MHz	150MHz	2.5GHz	9GHz	16GHz	21GHz
	5	400KHz	6MHz	150MHz	2.5GHz	10GHz	17GHz	23GHz
4%	1	50KHz	800KHz	25MHz	500MHz	3GHz	6GHz	13GHz
	2	75KHz	1.5MHz	40MHz	900MHz	4GHz	8GHz	15GHz
	3	125KHz	2MHz	50MHz	1GHz	6GHz	12.5GHz	18GHz
	4	150KHz	2.5MHz	60MHz	1.1GHz	7GHz	14GHz	20GHz
	5	150KHz	2.5MHz	60MHz	1.4GHz	7.5GHz	15GHz	22GHz
5%	1	15KHz	350KHz	9MHz	250MHz	2GHz	5GHz	11GHz
	2	40KHz	600KHz	10MHz	350MHz	2.5GHz	8GHz	14GHz
	3	50KHz	800KHz	18MHz	450MHz	4GHz	10GHz	17GHz
	4	90KHz	1MHz	20MHz	500MHz	5GHz	12GHz	19GHz
	5	80KHz	1MHz	20MHz	500MHz	5GHz	12.5GHz	20GHz

interval dependency over the PFET and NFET threshold voltages [56]. This means that lower WF decreases the NFET threshold, while higher WF will increase the NFET threshold, and vice-versa for PFET devices. Therefore, the ideal scenario would be with negative WFF for the PFET devices and positive WFF for the NFET devices. Though, the NFET term also depends on the β-ratio (ratio between the transistor emitter and base current) of the PFET and NFET transistors. Giving an estimate based on saturation and off-currents from [57], the NFET threshold voltage influence on the final hysteresis interval is almost 40% higher, in comparison to its counterpart.

As shown in Table 7, the only cases with considerable hysteresis worsening happens when the NFET WF is above 2%, while the subset showing improvements includes most of the possible scenarios. And since the hysteresis voltage will never be higher than the supply voltage, the average tends to the supply voltage value.

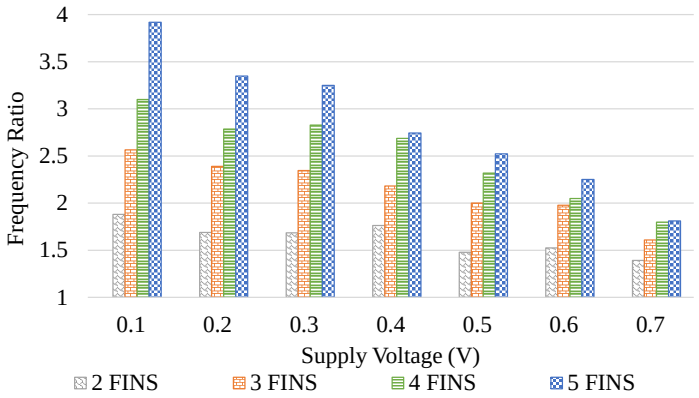

Fig. 17. Average frequency ratios between different layouts.

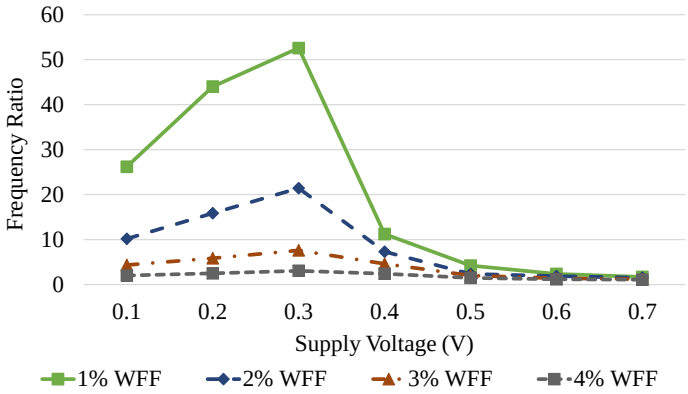

Fig. 18. Average frequency ratios between different WFF scenarios.

7 Conclusions

An analysis over multiple scenarios considering several levels of process variability, supply voltages, and transistor sizing was performed in order to identify the adequate number of fins and supply voltage for various kinds of applications prioritizing energy consumption and the minimization of deviations.

ST is a promising circuit for variability effects mitigation and enhancement of noise immunity being fairly applied on critical applications with tight reliability constraints. The results show that fewer fins can enable considerable energy reduction. On the contrary, for the ST robustness, a higher fin count will bring an increase in the on-current, bringing noise immunity improvements.

In performance results, it could be observed up to 16% and 44.65% maximum average increase and decrease in frequency, respectively, with differences between variability impact in the layouts rising alongside the supply voltage

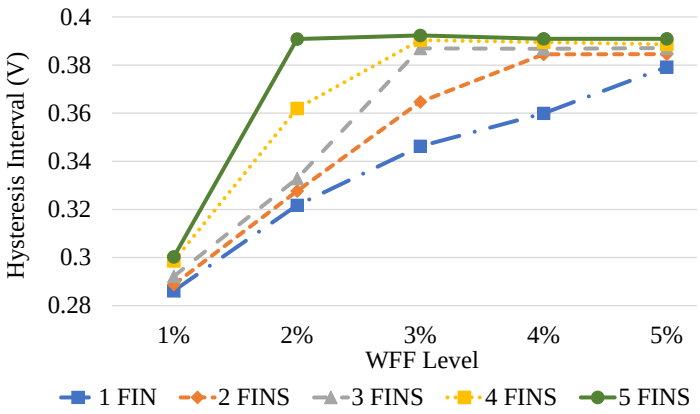

Fig. 19. Average of hysteresis interval increase over WFF scaling [60].

Table 7. Hysteresis interval ratio dependency over NFET and PFET workfunction [60].

NFET \ PFET	5%	4%	3%	2%	1%	0%	-1%	-2%	-3%	-4%	-5%
5%	**0.30**	**0.28**	**0.28**	**0.27**	**0.26**	**0.25**	**0.26**	**0.27**	**0.28**	**0.30**	**0.32**
4%	**0.46**	**0.46**	**0.55**	**0.54**	**0.54**	**0.54**	**0.55**	**0.56**	**0.57**	**0.59**	**0.61**
3%	**0.76**	**0.76**	**0.76**	**0.78**	**0.80**	**0.81**	**0.83**	**0.84**	**0.86**	**0.87**	**0.89**
2%	**0.88**	0.90	0.92	0.92	0.95	0.97	0.99	1.00	1.00	1.00	1.00
1%	0.93	0.94	0.97	0.99	1.00	1.00	1.00	1.00	1.00	1.00	1.00
0%	0.95	0.96	0.97	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00
-1%	0.95	0.96	0.99	0.99	1.00	1.00	1.00	1.00	1.00	1.00	1.00
-2%	0.96	0.97	0.99	1.00	1.00	0.99	0.99	0.99	0.99	0.98	0.98
-3%	0.95	0.97	0.99	0.99	0.99	0.99	0.98	0.98	0.98	0.97	0.97
-4%	0.93	0.94	0.97	0.97	0.96	0.96	0.96	0.95	0.95	0.95	0.94
-5%	0.93	0.94	0.96	0.96	0.96	0.95	0.95	0.94	0.94	0.94	0.93

value. The hysteresis intervals showed clear advantages over higher fin count and supply voltages with 10.76% and 25.26% better hysteresis. Considering energy consumption and variability, it was possible to achieve 24.84% and 14.44% decreases, respectively, with robust layouts taking advantage of a higher number of fins and a small decrease on the supply voltage while still maintaining very high frequencies of about 5GHz. A cost-benefit analysis was made as well, giving an additional option in order to achieve acceptable energy consumption and variability robustness.

For future works, we expect to investigate the effects of sizing on each feedback transistor on the ST circuit independently, introduce new designs and technology nodes into the analysis, take radiation effects, on top of the variability, into account and apply such circuits into more complex projects.

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