Offset-Compensation Systems for Multi-Gbit/s Optical Receivers

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Abstract. Offset compensation (OC) systems are indispensable parts of multi-Gbit/s optical receiver (RX) frontends. Effects of offset are addressed in this chapter. The analytical expression for the highest lower-cut-off frequency of the OC with minimum impact on the sensitivity is found. Existing OC solutions are discussed. Then, a novel mixed-signal (MS) architecture is introduced which uses digital filtering of the signal, and current-digital-to-analog converters to compensate the static offset in the limiting amplifier. In the transimpedance amplifier both static and dynamic offset are compensated. By using two feedback loops and a continuous tracking the presented solution offers more functionality than other existing MS architectures. Three RX implementations, with RC, switched-capacitor (S-C) and with the MS-OC architectures, in the same 28 nm bulk-CMOS are compared quantitatively with measurements. The presented MS design reaches a lower-cut-off frequency of under 9 kHz, a dynamic range of over 1 mA, 3.2 μA residual input offset-current and it is compensating the RX via two feedback loops. The presented system offers a higher flexibility and functionality in implementation, as well as a very good compromise between area, precision and performance over the commonly used RC-filter and S-C filter based solutions.

Keywords: Optical receiver, offset, offset compensation, mixed-signal control loop, residual offset, lower-cut-off frequency, transimpedance amplifier (TIA), limiting amplifier (LA).

1 Introduction

Optical links provide a cost- and power-efficient alternative to copper-based electrical interconnects for multi-Gbit/s ($\times$10 Gbit/s), short-range (<100 m) applications [1]. In board-to-board or rack-to-rack communications vertical-cavity surface-emitting laser (VCSEL) based multi-mode fiber (MMF) interconnect is the preferred choice over modulator with single-mode fiber. The reason behind is that the VCSEL driver power consumption is lower, voltages can be handled by CMOS technologies, while assembly and alignment efforts as well as costs are less in comparison to modulator-based transmission. In order to achieve the best performance at the lowest cost, full integration of the analog frontend, together with the digital data processing and switching core [2], and in future the photonic device as well [3], in the same highly scaled CMOS technology is aimed.

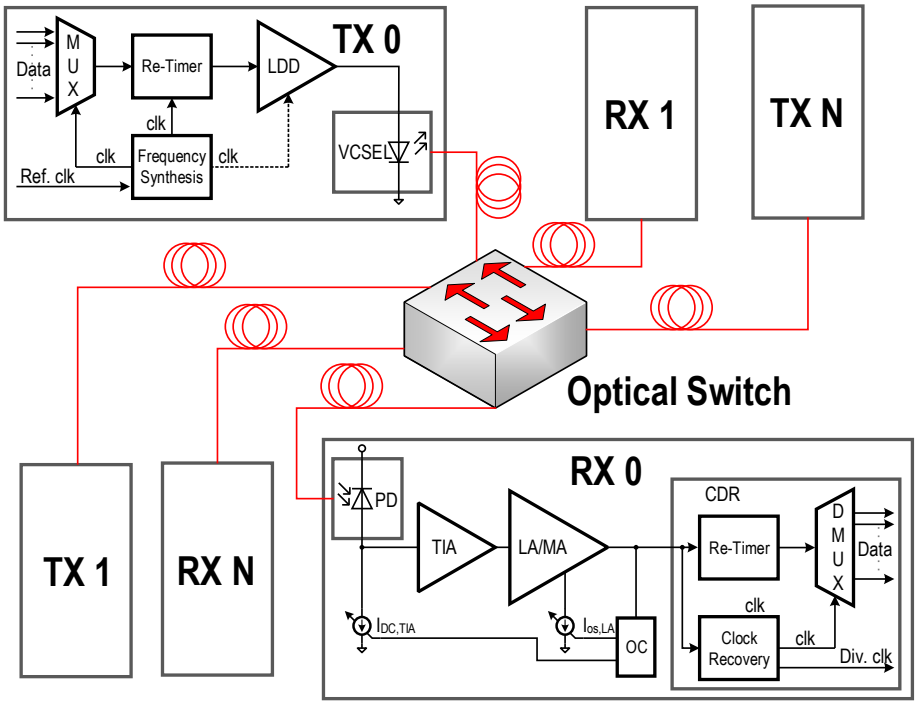


Fig. 1: Optical communication link in a network.

Such a short/medium range link is described in Fig. 1. It consists of VCSEL-based transmitters (TX). Parallel data streams at lower speed are multiplexed (MUX) to a single signal with high data-rate. It is then enhanced to a high amplitude by the re-timer, synchronized to the MUX by the frequency synthesis loop. The laser diode driver (LDD) transforms the digital signal into a high-power signal, with impedance matching to the VCSEL diode. Equalization can be used to cope with the bandwidth limitation of the VCSEL device [4], [5]. The optical signal reaches the receivers (RX) through MMF and optical switches. The RX itself uses a photo diode (PD) to convert the light into an electrical current. This is amplified and converted to a voltage by the transimpedance amplifier (TIA). The small voltage is further amplified and conditioned into a digital signal by the limiting amplifier (LA) or main amplifier (MA) with very high and sometimes variable gain. Next, the clock-data recovery (CDR) circuit extracts the clock from the signal and de-multiplexes (DMUX) the information in parallel streams, to the speed of standard digital logic. Additional circuits such as the offset compensation (OC) loop reduce the offset in the LA and sink the unwanted dc current of the PD.

Another field for short/medium optical links is in consumer electronics, with the spread of fiber-to-home. Its purpose is to provide very high speed internet at low cost. This can be achieved for example via passive optical networks (PON),

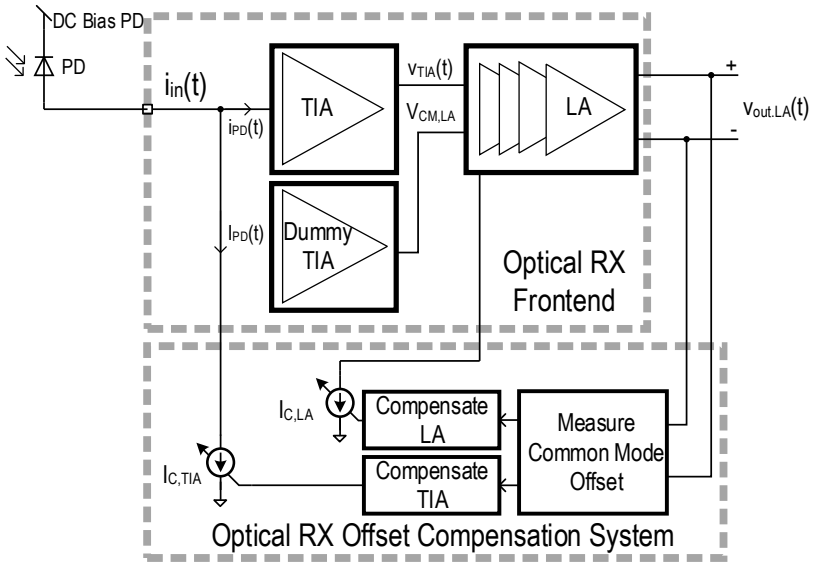


Fig. 2: Offset compensation system in an optical RX frontend.

where a passive optical switch is used instead the optical/electrical conversion, switching of the electrical signal then conversion back to the optical domain. This kind of network and system is illustrated in Fig. 1. It can be seen that for the same RX, TXs placed at different distances will transmit data packages in bursts of impulses. It results that different packages reach the RX with different optical power. This burst-mode RX needs to set the offset and common-mode compensation very fast so the data is received correctly. In this case analog loops reaction speed is too slow, therefore mixed-signal based compensation systems need to be used after taking the measures for the system to settle quickly.

2 State-of-art Offset Compensation

The received signal in VCSEL-transmitter based links suffers from a strong dc component created by the limited extinction-ratio of the optical signal [6]. This current needs to be removed by the RX, which needs to deal with variations of optical power and mismatch created offset as well. Little attention is given in the available literature to the offset and dc-current compensation (OC) systems in optical RXs. In Section 3, OC systems and the most important parameters of the design process are addressed. An analytic expression for the maximum lower-cut-off frequency is obtained for a given data rate (DR) bit pattern and allowed sensitivity deterioration [7]. At present, the most common OC system is based on RC low-pass filter (LPF) [8–12], that suffers from several drawbacks such as extremely high area, power consumption dependent residual offset, stability and fixed lower-cut-off frequency. Some of these issues are dealt by the

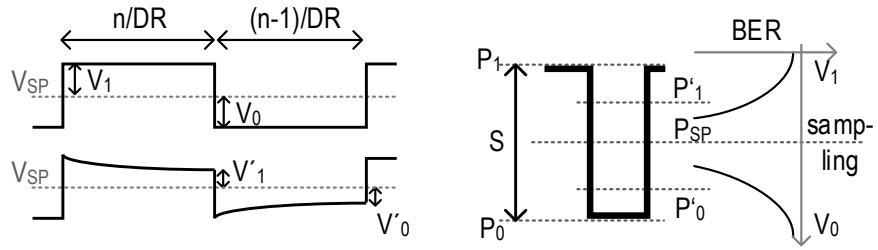
switched-capacitor (S-C) LPF based systems [8,13,14]. Their area is significantly smaller and the lower cut-off frequency is adjustable. Section 3 gives the analitical dependency between the low-pass frequency of the LPF and lower cut-off frequency of the RX. These conventional architectures are discussed in Section 4. A fully flexible system can be implemented in a digital CMOS process by using mixed-signal (MS) control loops with digital-to-analog converters (DAC). Such OC system was implemented in [3] using a 7 bit current-DAC (IDAC) which is used for calibration, compensating for the static offset.In [2] an IDAC with successive approximation register (SAR) is used to calibrate for the dc current at the input of the RX at every burst cycle.

A novel MS OC architecture is introduced in Section 5 that uses digital filtering and compensates with an IDAC the static offset of the LA stage of the RX and a second IDAC with SAR algorithm reduces the dc current at the input of the TIA. Then, this second IDAC, in contrast to [2] continuously tracks and compensates the offset during operation. This architecture was implemented and presented briefly in [15]. In [16] further details regarding the digital algorithms, the IDACs, measurements and comparison of the different systems is described. This chapter reveals further theoretical and modeling issues, and extends the scope of MS systems into burst-mode RXs for PONs. A 28 nm bulk-CMOS process is used to implement a RX with the proposed MS OC system [15], one with RC-LPF OC [9] and one with the S-C OC [14]. Advantages of the MS OC over the other two systems are discussed. Superiority of the proposed architecture is proven when measurement results are compared in Section 6.

3 Offset Compensation in Optical Receivers

The optical RX system, as depicted by Fig. 2, consists of the RX frontend and the OC system. The useful signal $i_{PD}(t)$, part of $i_{in}(t)$, is a current generated by the PD amplified by the TIA and converted in a voltage $v_{TIA}(t)$. A dummy TIA provides the common mode at the differential input of the LA $V_{CM,LA}$. Several LA stages further amplify the signal into $v_{outLA}(t)$ that will go to the next blocks in the signal processing chain [13] .

Process spread and mismatch causes static offset in the LA [12]. At the TIA input $i_{in}(t)$ also contains a dc current which can slowly change with time, $I_{PD}(t)$ caused by the finite extinction ratio of the transmitter laser diode [6]. This causes $V_{TIA}(t)$ to drift. Furthermore, temperature variation and changes in the input optical power will cause dynamic offset seen as difference between $V_{CM,LA}$ and $V_{TIA}(t)$. As the RX chain, especially the LA, has a very high gain, a small offset in the RX can cause saturation of the output stages, thus result in the impairment of functionality. For this reason an OC system is used that has the block diagram depicted by Fig. 2. The difference between the common-mode of the two output polarities is measured. Then, $I_{C,LA}$ compensates for the static offset of the LA. Meanwhile $I_{C,TIA}(t)$ sinks the dc current coming from the PD, $I_{PD}(t)$, which also compensates for the variation of optical power at the input.



(a) Effect of a low cut-off frequency on a *n* long bit sequence.

(b) Relation of sampling level, sensitivity, P_1 and P_0 to the BER.

Fig. 3: Low cut-off frequency effect on the signal, sensitivity and BER.

Offset between the common modes of the TIA and dummy TIA is also reduced by $I_{C,TIA}(t)$.

The offset compensation loop, which cancels the dc component of the signal behaves as a high-pass filter in the signal path. Not only the dc component is extracted, but in reality there is a low-pass frequency, mainly limited by technological considerations, therefore a significant amount of components in frequency domain are canceled. This causes a high-pass effect called "dc-wander" [17]. Figure 3a shows how an n-bit long run of *1*'s with DR and V_1 amplitude will decrease to V_1'. The same can be observed for a long run of *0*'s. In order to avoid this, either the number of consecutive same-state bits (run length) or the lower cut-off frequency f_{LCO} has to be reduced [17]. Since the run length is defined in the transmission standard, the f_{LCO} needs to be decreased accordingly.

A common signal-patern standard used in wire-line communications is the pseudo-random bit sequence (PRBS) with the length of $2^n - 1$ bits. A PRBSn has a run length of n *1*'s and *n-1 0*'s. For simplicity, however n will be used for both *1*'s and *0*'s.

The decay of voltage from $V_{1/0}$ to $V'_{1/0}$, shown in Fig. 3a can be expressed as

$$V'_1 = V_1 \cdot \exp\left(\frac{-2\pi n_1 f_{LCO}}{DR}\right). \tag{1}$$

The sensitivity, S is one of the most important measures of a RX and is the smallest input signal power that can be amplified error-free. In optical communications this signal is quantified by the optical modulation amplitude (OMA) of the signal. As it can be seen in Fig. 3b, $S = P_1 - P_0$. The $P_{SP} = (P_0 + P_1)/2$ in Fig. 3b is the level with the lowest bit error-rate (BER), therefore it is chosen as the sampling level and is meanwhile the common-mode or symmetry level of the signal $P_{CM} = P_{SP}$. So, dc-wander causes P_1 to decrease into P'_1, while P_0 increases to P'_0, thus S to worsen with the long *0* and *1* run, causing an asymmetry by shifting P_{SP}, thus a "decision offset" [18]. The new sensitivity will be now $S' = P'_1 - P'_0$. A power-penalty of the sensitivity PP_S can be defined, that accounts for dc-wander effect on both levels

$$PP_S = S - S' = P_1 - P_0 - P'_1 + P'_0. \tag{2}$$

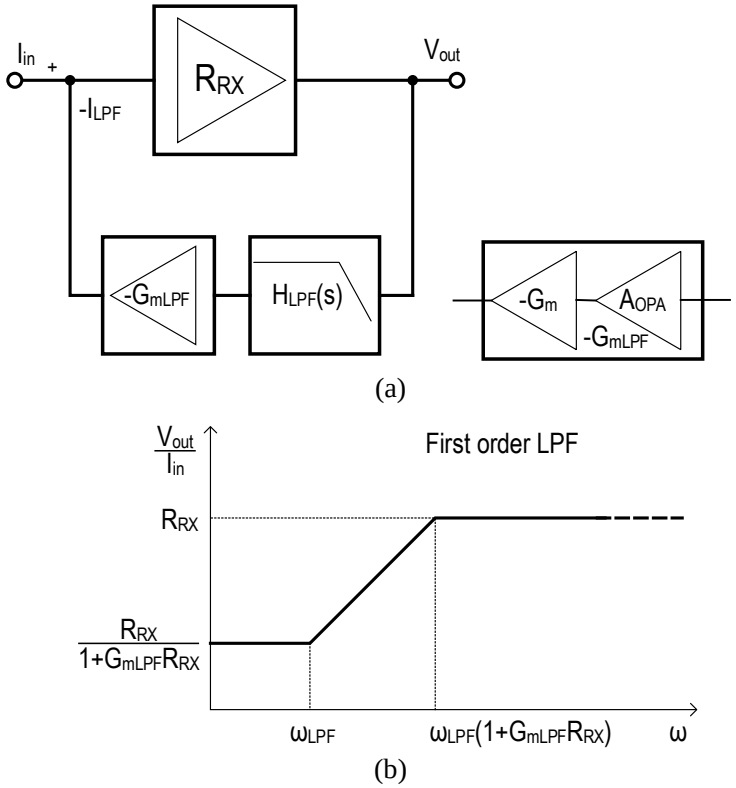


Fig. 4: Lower cut-off frequency f_{LCO} (a) System view and (b) calculation for a first order LPF.

By fixing $P_{SL} = P'_{SL}$, thus the sampling takes place at the same level in both cases, results

$$P_1 - P'_1 = P_0 - P'_0. \tag{3}$$

Introducing (3) into (2) the power penalty can be further written as

$$PP_S = 2(P_1 - P'_1). \tag{4}$$

To express P'_1, equation (1) is used, considering a fixed resistance. Next, $n_1 = n_0 = n$ is considered for simplicity in (1). This is introduced in (4) so the power penalty can be expressed in dB $PP_S(dB)$ as

$$PP_S(dB) = 40\pi \frac{n f_{LCO}}{DR} \log_{10} 2e. \tag{5}$$

In the following, a PRBS31 signal is used to evaluate the performance of RXs and $PP_S < 0.01$ dB is aimed, meaning an insignificant sensitivity deterioration. With equation (4), f_{LCO} of 70 kHz can be calculated for a DR of 20 Gbit/s.

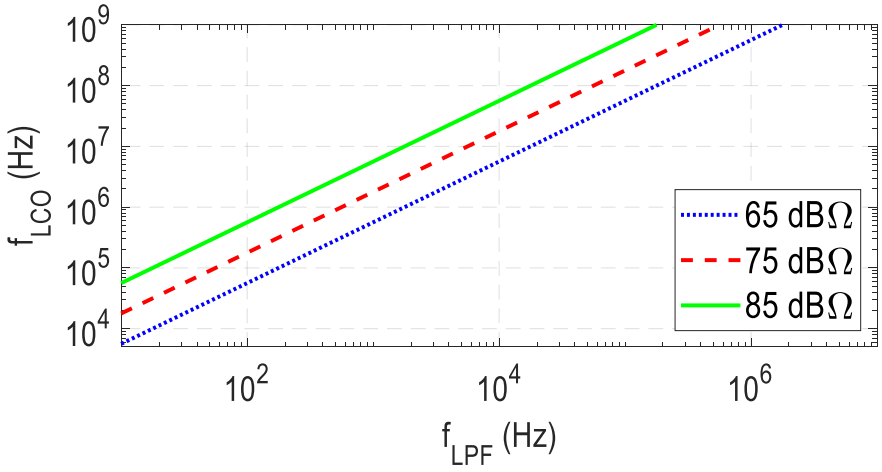


Fig. 5: Lower cut-off frequency f_{LCO} dependence on f_{LPF} at different RX gains.

It can be concluded that an OC system is needed for an optical RX in order to ensure its error-free functionality. Furthermore, the lower cut-off frequency must be low enough so the sensitivity at an error-free detection is not degraded with a given run-length of the input data at the desired DR.

4 Conventional Low-pass Filter Based Offset Compensation

The most straightforward way to implement an OC loop is by using a LPF in a negative feedback loop, as depicted by Fig. 4a. The RX with transimpedance gain of R_{RX}, output voltage V_{out} is passed through the high-pass filter with output voltage $H_{LPF}(s)$. This has a negative transconductance gain of output voltage -G_{mLPF} and creates a feedback current -I_{LPF} added to I_{in}. -G_{mLPF} will be implemented practically as shown in Fig. 4a from an operational amplifier (OPA) with voltage gain A_{OPA} and a transconductance -G_m, for instance a current-sink transistor. The loop can be described with as

$$V_{out} = R_{RX}\left[I_{in} + V_{out} G_{mLPF} H_{LPF}(s)\right]. \tag{6}$$

From equation (6) the lower cut-off characteristic $H_{LCO}(s)$, dependent on the LPF can be expressed as

$$H_{LCO}(s) = \frac{V_{out}}{I_{in}} = \frac{R_{RX}}{1 + R_{RX} \cdot G_{mLPF} H_{LPF}(s)}. \tag{7}$$

Equation (7) gives a generalized formula for $H_{LCO}(s)$. When a first-order LPF is used, such as an RC LPF the transfer characteristic can be expressed in a more specific manner, such as depicted in Fig. 4b. A zero is created in $-\omega_{LPF}$, while

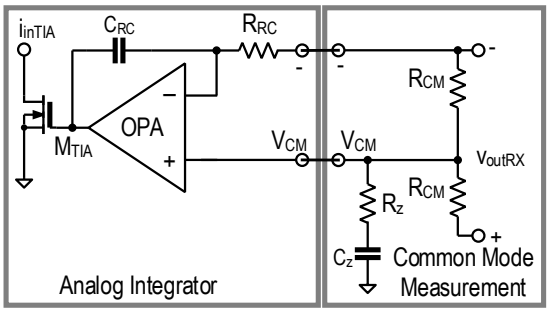


Fig. 6: Conventional RC low-pass filter based offset compensation schematic.

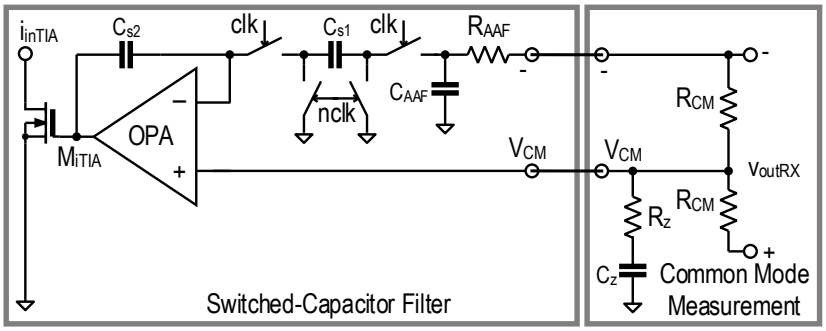


Fig. 7: Conventional S-C low-pass filter based offset compensation schematic.

a pole appears in $-\omega_{LPF}(1 + R_{RX} \cdot G_{mLPF})$. The dc offset and low frequency signal will be suppressed to $R_{RX}/(1 + R_{RX} \cdot G_{mLPF})$ leading to the conclusion that G_{mLPF} should be made as high as possible. However, if f_{LCO} is expressed depending on f_{LPF}

$$f_{LCO} \approx R_{RX} \cdot G_{mLPF} f_{LPF}, \tag{8}$$

it can be seen that increasing G_{mLPF} results in increasing f_{LCO} that will require larger LPF elements in order to keep the same f_{LCO}. This is illustrated in Fig. 5, where it can be seen how changing f_{LPF} impacts f_{LCO}. The simulation is done with different, common RX transimpedance gains of 65, 75 and 85 dBΩ. Gain in the feedback is kept constant, with a customary A_{OPA} of 50 dB and 1 mS one-transistor current sink G_{mLPF}.

It can be concluded from Fig. 5 that f_{LPF} needs to be significantly lower than the required f_{LCO} resulting in extremely large elements for the filter, implicitly a very area inefficient circuit topology.

As the lower-cut-off frequency needs to be in the kHz domain, the LPF needs a capacitor in the nano-Farad region, which cannot be realized on-chip. This method, although still found in [1] has become rather obsolete. A simple on-chip RC filter is used in [19]. However, it needs a 13 MΩ resistor and 150 pF capacitor which occupy an unacceptably large area for the highly scaled RX designs from

today. A very common implementation [9–12] is the active RC filter where the Miller effect is used to multiply the capacitance to $C_{Mill} \approx A_{OPA}C_{RC}$ as also depicted by Fig. 6. This solution offers a low complexity circuit on a reasonable area. The cut-off frequency of the LPF can be approximated as

$$f_{LPF,RC} = \frac{1}{2\pi R_{RC} C_{RC} A_{OPA}}. \tag{9}$$

The biggest disadvantage of this method is that the f_{LCO} is fixed by the resistor and capacitor and need to be sized, according to equation (5) to the lowest DR and longest run length which results in an increased area.

This disadvantage can be overcome by implementing a tunable filter. The S-C filter has a clear area advantage over the RC LPF thus it has been chosen in [8] and [13]. The switches and C_{s1} in Fig. 7 emulate a large resistor. The cut-off frequency of the LPF can be expressed as

$$f_{LPF,S-C} = f_{clk} \frac{C_{s1}}{C_{s2}}. \tag{10}$$

It can be seen in (10) that $f_{LPF,S-C}$ can be adjusted with f_{clk}. A S-C LPF needs additionally an anti-aliasing filter (AAF) with a cut-off frequency of at least $f_{clk}/2$ [8]. This results in a compromise that needs to be done when choosing the clock frequency, C_{s1}/C_{s2} ratio which can be limited by the smallest capacitor in a given technology and the accuracy of the ratio when the smallest value is used and finally f_{AAF} as this additional filter directly impacts the area needed by the OC loop.

A major drawback of LPF based offset compensation loops is the residual offset. For the conventional systems from Fig. 6 and 7 residual offset current $I_{os,rez}$ can be expressed as

$$I_{os,rez} = \frac{2I_{os,RX}}{A_{RX} \cdot A_{OPA}} - \frac{2V_{os,OPA}}{A_{RX} \cdot R_{T,RX}}. \tag{11}$$

Equation (11) shows how $I_{os,rez}$ is influenced by several factors. In order to decrease this unwanted current the gain of the OC loop, namely A_{OPA} needs to be as high as possible. This can cause stability issues as well as burn a significant amount of power.

5 Novel Mixed-signal Offset Compensation

5.1 System Considerations

An offset compensation with digital core is proposed. Figure 8 shows the block diagram of the mixed-signal OC loop. An RC AAF isolates the output of the RX from the clock of the digital core. f_{AAF} is chosen 2 MHz. A comparator follows, which decides if there is a difference between the negative RX output $-$ and V_{CM}. The comparator results are accumulated in a digital integrator with 1024

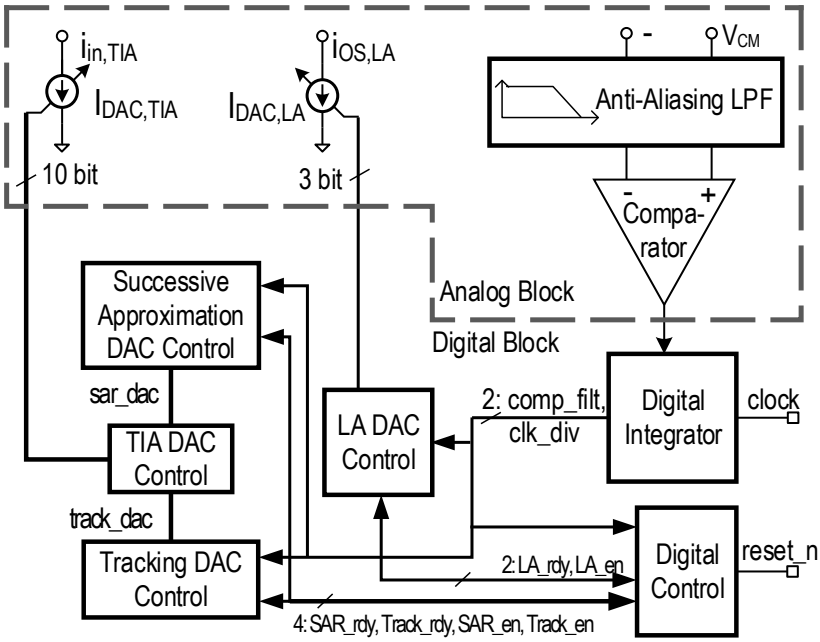


Fig. 8: Block diagram of the mixed-signal offset compensation system.

samples. The result *comp_filt* indicates whether the majority of the samples was positive or negative. By building an average, the high frequency components are suppressed similar to a conventional LPF. This is described by by the signal flow in Fig. 9a. This block divides the clock as well, so for every decision of *comp_filt* there is a clock edge on *clk_div*.

5.2 Digital Design

The following blocks are controlled by the finite state machine (FSM) or digital control block. Figure 9b shows the state diagram of the FSM. After the reset signal *rst_n* the 3 bit *LA DAC* will overcompensate roughly the offset in the LA, until *comp_filt*=1. Then, after the *LA_rdy* signal the FSM hands over control to the SAR TIA DAC. As visible in Fig. 9b, the *SAR TIA DAC Control* will use the SAR algorithm to compensate for the input offset current and dc current generated by the average light power of the PD. After 10 bits the process is handed over to the *Track TIA DAC Control*. Figure 9c shows how the tracking works. When the current at the input changes, first the direction is detected, if the current increased the DAC will be stepped one bit up, if it decreased one bit down, until full compensation is achieved. In case of reset *rst_n* the FSM returns to the *LA_DAC* state. The common-mode offset is continuously tracked and compensated by increasing or decreasing the current at the TIA DAC in a thermometric manner.

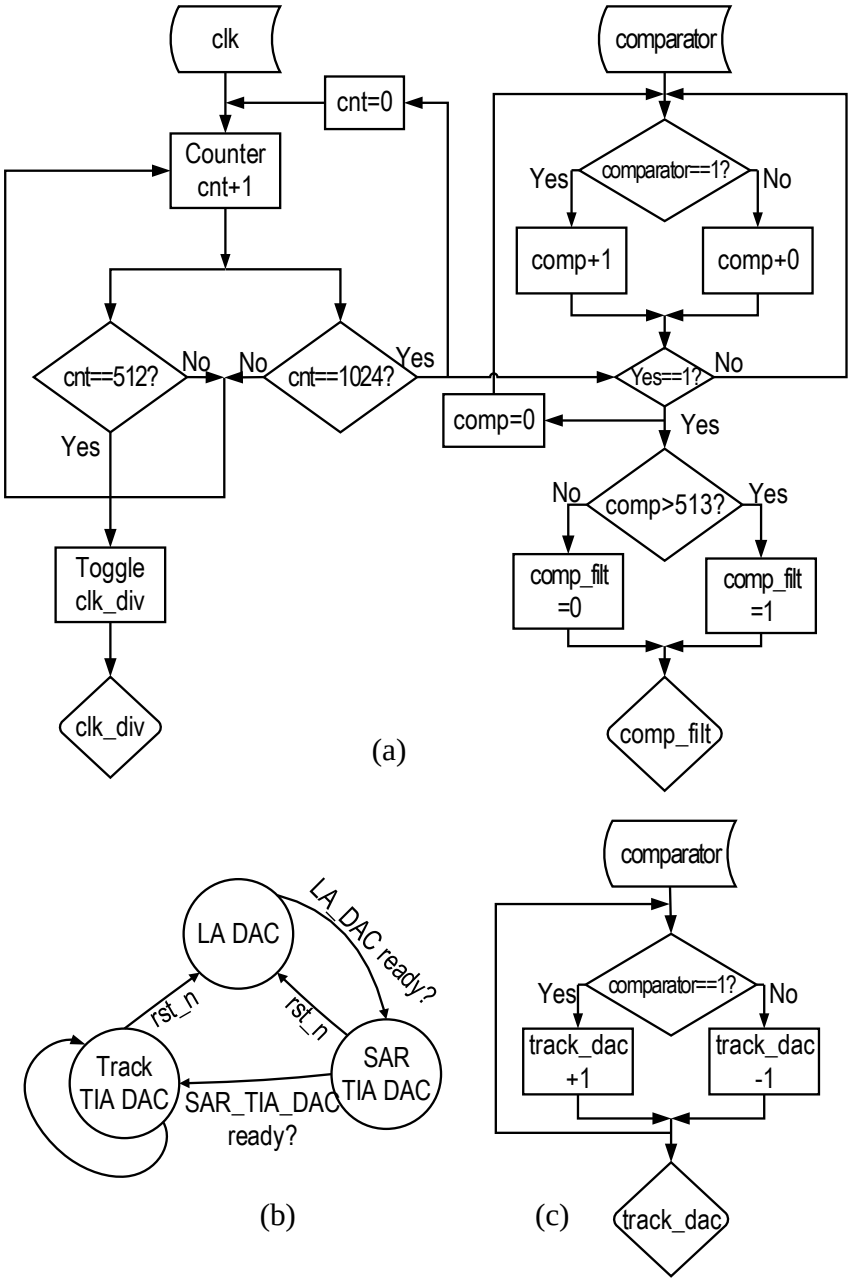


Fig. 9: Mixed-signal offset compensation system: (a) Digital integrator signal flow; (b) Finite-state-machine; (c) Tracking algorithm flow.

The digital integrator and the controlling state machine were synthesized using a custom 14-Track 1V standard cell library. The digital library consists of

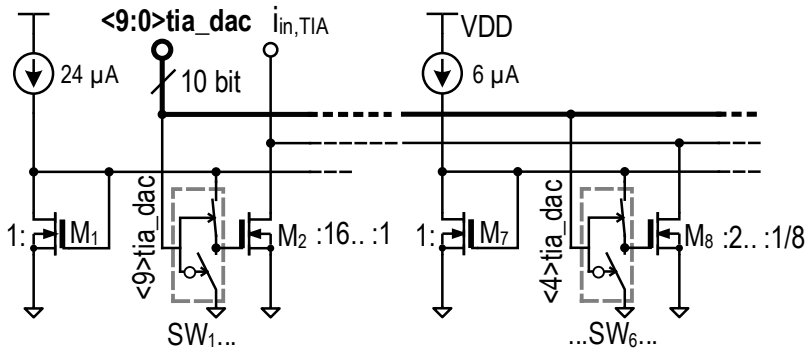


Fig. 10: Schematic of the TIA current DAC (IDAC TIA).

133 standard cells and its design is described in [20]. The lack of prior hardware testing was one of the reasons to keep the clock frequency low at 2 MHz. With a hardware proven library, the clock frequency could be set significantly higher, which would allow significantly faster convergence.

5.3 The Digital-to-Analog Converters

The schematic of the IDAC TIA is shown in Fig. 10. It is a binary weighted DAC split in two, sub-DACs. This is done in order to maintain a reasonable aspect ratio between very large and very small transistors, thus maintaining a reasonable matching. It follows, that 24 μA are injected into the reference M_1, while M_7 sinks 6 μA. Turning on and off the current sources is done by toggling between the reference voltage or ground of the gate of transistors M_2 to M_6 and M_8 to M_{12}. IDAC LA is implemented in a similar way with only 3 bits.

5.4 Scalability

A major motivation for the MS approach is its scalability. The lower cut-off frequency of the loop can be easily adjusted by means of the digital clock frequency. While only low-frequency digital clock has been implemented out of reliability concerns, clock frequencies in the order of GHz are feasible for hardware proven standard-cell libraries. Since the dynamic properties of the proposed offset compensation loop are proportional to the clock period, there are extremely high prospects for improvements of the transient behavior. With additional changes to the successive approximation algorithm, a convergence in the order of 20 ns can be achieved as shown in Fig. 11 in comparison with a conventional RC-low pass filter with the low cutoff frequency of 70 kHz. Such dynamic behavior would be suitable for burst-mode operation.

The digital circuits can be easily modified and extended without major design effort, unlike the analog implementations. Similarly, the porting to a different technology is easier and more reliable, since the behavior of the loop is

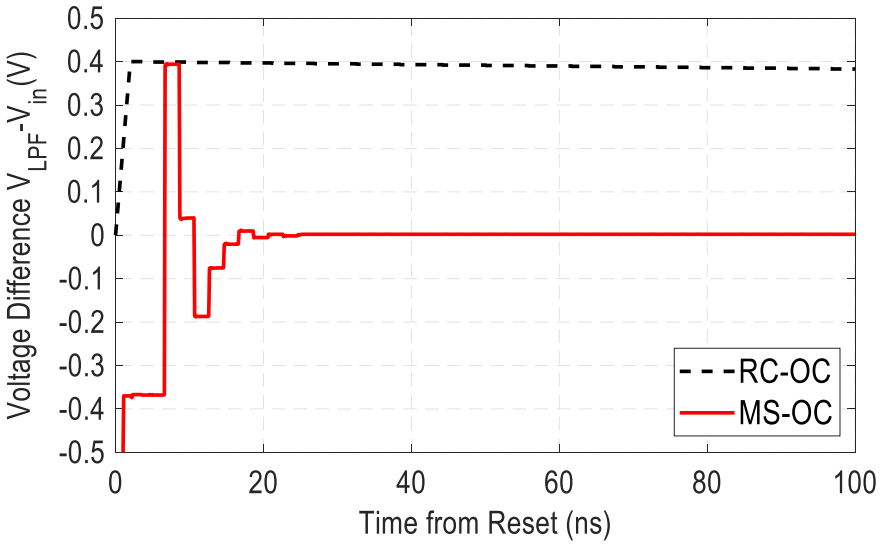


Fig. 11: Simulated turn-on time with an RC and MS loop with fast SAR algorithm.

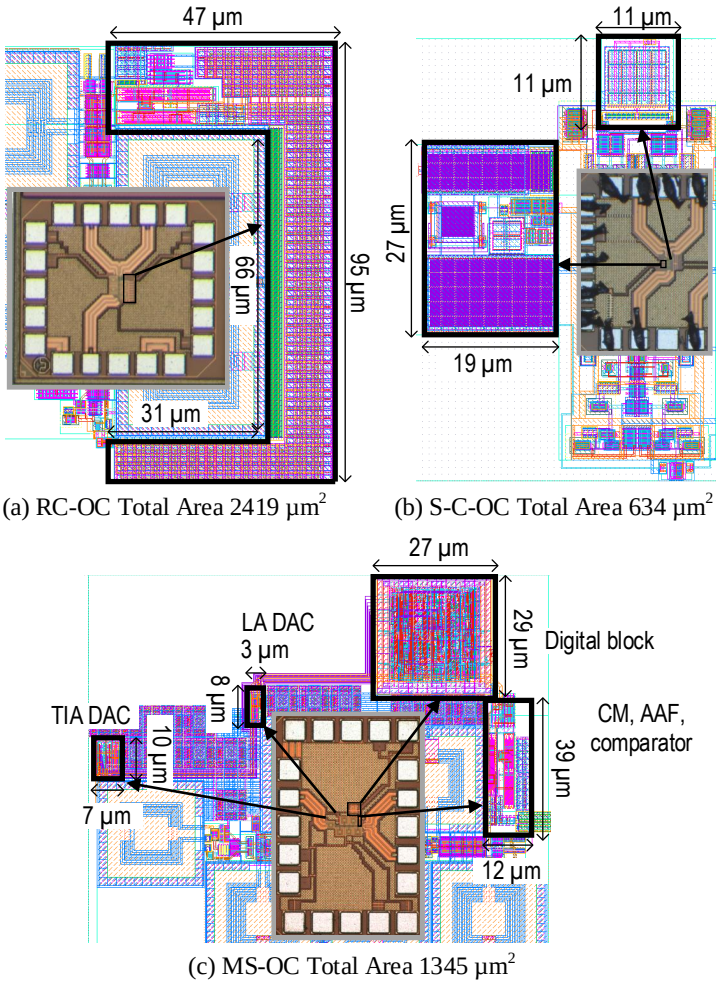
determined by the clock frequency and RTL description, which are technology-independent.

On the other hand, the presented approach shares the challenges typical for system-on-a-chip (SoC) designs. A wider tool-set as well as standard cell IP are required for the design. Supply separation and supply noise rejection might be gradually predominant with increasing clock frequency of the OC loop and the complexity of the digital block.

5.5 Burst-Mode Operation

Another argument supporting MS approach to OC is their suitability for burst-mode operation and therefore usage in PON systems as described in Section 1. Adaptive systems are another oportunity for burst-mode receivers [15]. In the current state-of-the-art, optical transceivers usually operate in full speed mode constantly. While the VCSEL cannot be completely turned off due to long power-on time, considerable power-savings can be achieved by powering down other parts of the transceiver. As shown in [21] and [22], up to 50 % power consumption can be saved by disabling parts of opto-electronic transceivers while maintaining acceptable power-on time for burst-mode operation.

Fast power-on times are required to allow acceptable latency and avoid the necessity for large memories to store the data during the power-up time. The settling time of a conventional OC loop is inversely proportional to the lower-cut-off frequency of the LPF and therefore results in considerable wake-up time. The bandwidth of a MS signal OC loop can be controlled dynamically using its



(a) RC-OC Total Area 2419 µm^2 (b) S-C-OC Total Area 634 µm^2

(c) MS-OC Total Area 1345 µm^2

Fig. 12: Offset compensation implementations: (a) RC filter, (b) S-C filter (c) Mixed-signal.

FSM to allow fast settling at wake-up as well as sufficient dc rejection during regular operation. While a dynamic LPF adjustment can be achieved using analog techniques as well, as shown in [2], the MS loop also has better retention and can maintain its value with minimum power consumption as long as supply is active.

6 Measurements and Comparison

For comparison of the three systems, two previously implemented RX chips, one with RC filter [9] and one with S-C filter [14] and a new design with mixed-signal

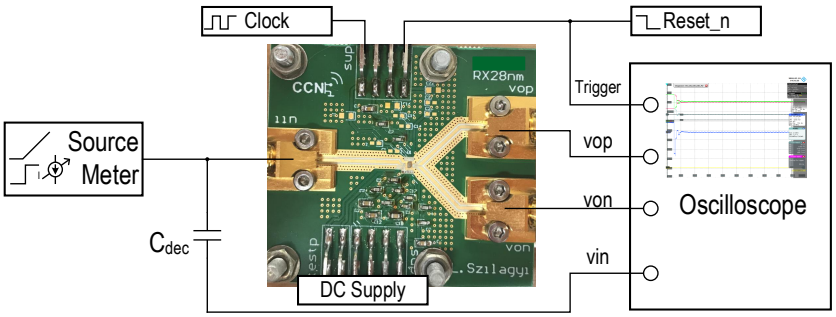


Fig. 13: Measurement setup.

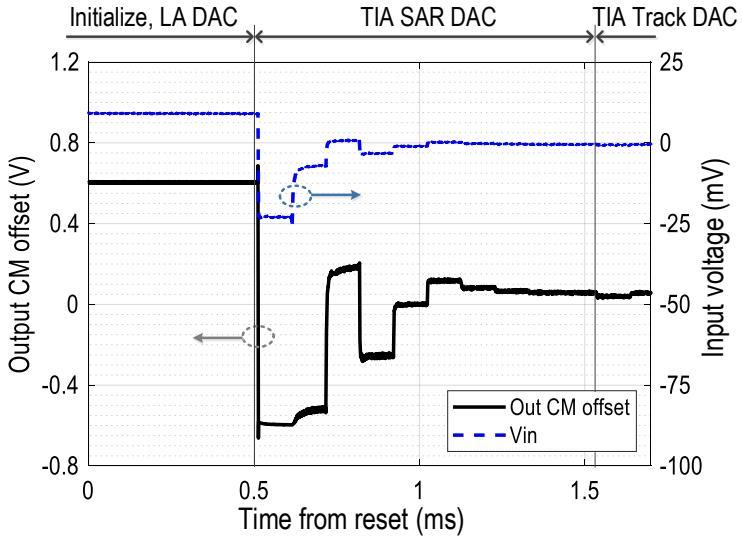


Fig. 14: Oscilogram of the MS OC, output CM offset and input signal.

OC system [15] were designed and fabricated in the same 28 nm bulk-CMOS digital process.

Figure 12a shows the RC filter based OC system. A capacitor C_{RC} of 15 pF and R_{RC} 3.6 MΩ are used as in the schematic from Fig. 6. These large passive devices increase the area of the RC-LPF based OC to over 2400 μm^2. The S-C-LPF OC system implementation is shown in Fig. 12b. The corresponding values to the components in Fig. 7 are C_{AAF} of 2.2 pF and R_{AAF} 400 kΩ for the AAF and C_{s1} of 35 fF, C_{s2} of 4.4 pF for the SC LPF. f_{clk} is 5 MHz in this case. The total area is only 634 μm^2. The middle value of 1345 μm^2 is needed for the MS-OC system from Fig. 12c. The digital block occupies 783 μm^2, the rest is occupied by the AAF, comparator and DACs.

The setup in Fig. 13 is used to show the functionality of the MS-OC system. For stable measurements the chip is bonded to dc and signal connections on a

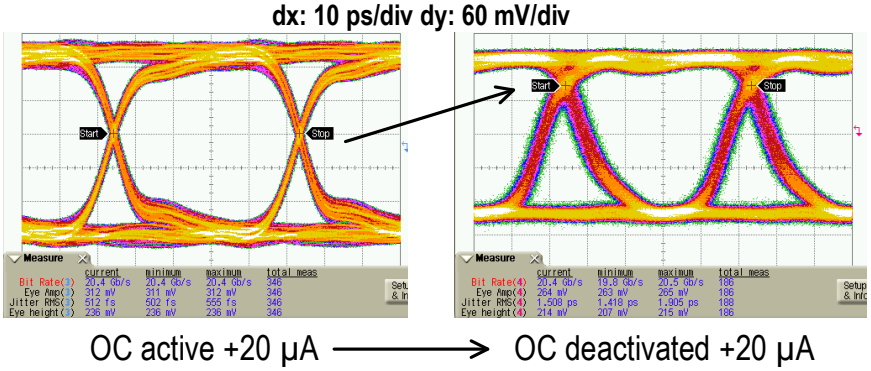


Fig. 15: Eye diagram at 20 Gbit/s +20 μA offset with OC active and de-activated.

PCB. A 5 MHz square wave clock with 50 % duty cycle and 1 V amplitude is used for the following measurements. The *reset_n* is used as a trigger for the oscilloscope, that visualizes the output and input voltages as well. Next, a source meter is used to inject a current ramp or step.

In order to measure the residual offset, a dc current of 100 μA is injected in the input. The output common-mode offset $V_{os,CM,out} = V_{vop} - V_{von}$ are visualized and measured in Fig. 14. At the start of the sequence more than 600 mV initial offset is measured at the output. Until around 0.2 ms the digital block is initialized and the LA DAC started. It can be seen that after bit 2, the offset changes its sign. The OC procedure is handed over to the *SAR TIA DAC*. Then, the SAR algorithm can be clearly seen until around 1.6 ms. Finally, the TIA DAC toggles the current at the input by the least significant bit up/down to sense a change on the dc current. The final average output offset voltage is 18 mV. Knowing the RX has a transimpedance gain $R_T(\text{dB}\Omega)$=74 dBΩ [15], the residual, input-referred offset current of 3.2 μA can be estimated.

Next, the effect of offset on the transmitted signal and functionality of the OC is demonstrated. Additionally to the setup in Fig. 13 a PRBS signal current with 20 Gbit/s is injected to the input of the RX. The outputs are connected to a high-speed sampling oscilloscope. The source meter will inject 20 μA of dc current. It can be seen in Fig. 15 that a correctly balanced eye diagram can be captured at the output of the RX. Next, the clock is deactivated. It can be seen that already such a small current causes the crossing point of the signal shifting up by more than 100 mV. This results in a signal that cannot be detected error-free anymore. This experiment simulates the changes in optical power of the received signal. Furthermore, it demonstrates the necessity of an OC system as the correct functionality of the presented circuit.

The second important comparison point is the f_{LCO}. For this measurement a Rhode & Schwarz, ZVL6 network analyzer with 9 kHz lowest frequency is used. A short-open-load-through calibration is done with a standard kit. Figure 16 shows the transfer functions of the three RX up to 1 MHz. Since the chips have different gain, the normalized transfer function is used. It can be seen that the

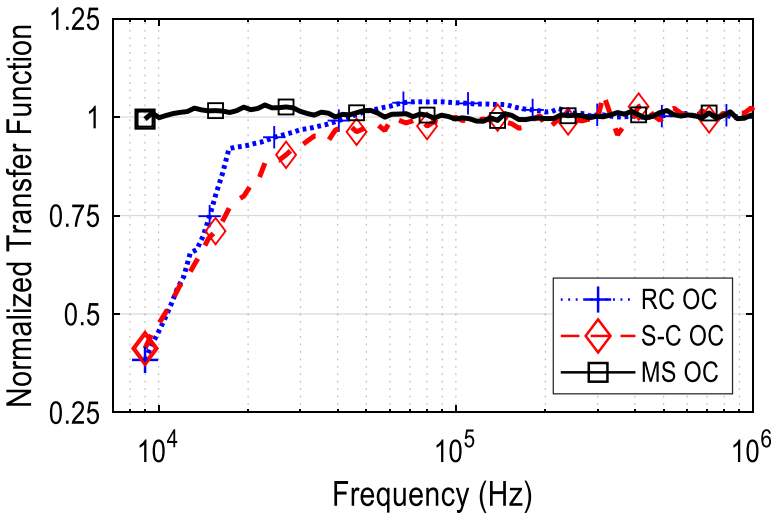


Fig. 16: Measurement of the lower cut-off frequency f_{LCO}.

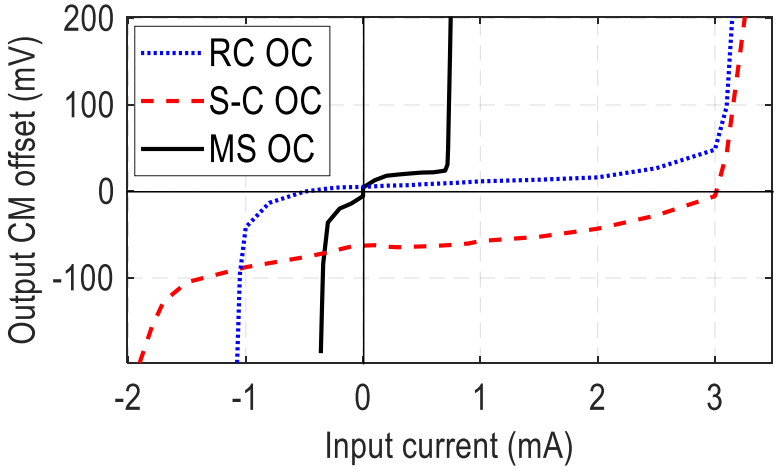


Fig. 17: Measured dynamic range of the OC architectures.

RX using RC and S-C LPF OC system have a similar f_{LCO} of approximately 20 kHz (with f_{clk} of the S-C LPF of 5 MHz). The MS OC system has on the other hand f_{LCO} which is much lower than the instrument can measure, when f_{clk}=5 MHz. This is around 4.9 kHz.

The dynamic range of an OC loop (I_{DR}) can be defined as the difference between the highest and lowest dc current that can be applied at the input which will cause a negligible offset voltage at the output, $V_{OS,CM,out}$. A value of 10 % of the single-ended output swing is chosen as limit for offset, that is approximately

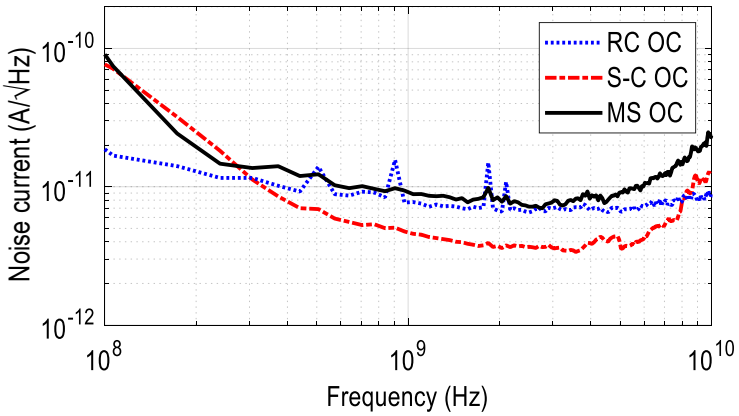


Fig. 18: Measurement of the input referred noise current.

30 mV for the MS OC. This parameter depends on the size of the compensation current source, or in case of the MS-OC, on the dynamic range of the IDAC. It was measured using the setup from Fig. 13, by injecting a slow current ramp in the RX. The output CM offset exceeded 30 mV for 0.72 mA input current, that corresponds to 1.58 dBm optical power with a 0.5 A/W responsivity PD. By using a second IDAC (LA DAC), that has an opposite sign to the TIA DAC, negative input current of up to -0.34 mA can be compensated. Figure 17 shows the dynamic range measurement results. It can be seen that, although the S-C OC has the highest dynamic range, its residual offset is large, -49 mV at the output. In case of the MS OC, the I_{DR} can be adjusted precisely according to the design requirements by increasing the LSB current or the number of bits for the TIA IDAC, meanwhile for the other two architectures only a vague forecast can be made. In addition, these implementations of the LPF based systems use a complementary PMOS to M_{iTIA} in order to compensate also negative currents. By this, a constant quiescent current of about 1 mA is constantly drawn from the supply that is present even if no dc current from the PD is sourced. The MS OC on the other hand does not have this disadvantage.

Although the noise spectral density (NSD) depends strongly on the gain and bandwidth of the complete RX, the input referred noise current of the three receivers was measured, plotted in Fig. 18 and the NSD calculated in Table 1. It is found that by using a proper AAF, clocked OC loops (S-C and MS) have no negative influence on the noise performance and input sensitivity of the RX.

Table 1 compares the three OC systems discussed in this chapter. It can be seen that the MS system offers the best trade-off between area, f_{LCO} and residual offset current. The RC and S-C LPF based OC in these implementations compensate the offset only at the input of the TIA and for the dc input current. On the other hand the proposed MS OC reduces the static offset of the LA in addition to the TIA input and dc current at the input. The biggest advantage of the proposed system is its flexibility. By reducing the sample number at the

Table 1: Comparison of the offset compensation systems.

Parameter	Unit	[9]	[14]	This work [15]
Architecture		RC LPF	S-C LPF	MS
Area	(μm^2)	2419	634	1345
$I_{os,res}$	(μA)	1.7	24.4	3.2
I_{DR}	(mA)	3.3	3	1.06
f_{LCO}	(kHz)	20	20	< 9
f_{LCO} adjustable	y/n	no	yes	yes
NSD	(pA/$\sqrt{Hz}$)	73	43	84
Compensated Blocks		TIA	TIA	TIA & LA

digital integrator, the loop speed can be increased so the system can be used in burst-mode RX as in [2].

7 Conclusion

The function of offset compensation in optical receivers is addressed. The lower-cut-off frequency is defined and a calculation method is given for the highest frequency that does not impact the RX performance. An analytical relation between the lower cut-off frequency and low-pass frequency for filter-based systems is defined. Therefore, this chapter presents a complete modeling tool for offset compensation in optical receivers. Existing offset compensation solutions are discussed. Then, a novel mixed-signal architecture is introduced which uses digital filtering of the signal, an IDAC to compensate the LA, and a second IDAC for the TIA. The second IDAC first reduces static offset with the SAR algorithm and then continuously tracks and compensates the offset at the input of the TIA. The presented solution differs from other previous implementations that it reduces the offset using two DACs and from other mixed-signal solutions that it not only calibrate for the static offset but continuously tracks the changes in offset and compensates them. The system is extended for burst-mode receivers suitable for PON systems.

The quantitative differences to the commonly used architectures based on RC-filter and S-C filter are shown also by comparing measurements on three RX implementations each with one of the mentioned offset-compensation system, in the same 28 nm bulk-CMOS technology. The comparison is done in terms of area, residual offset current, dynamic range, lower cut-off frequency and noise spectral density. System considerations as adjustable lower cut-off frequency and the compensated RX blocks are also taken in consideration. It is found that the presented system offers a higher flexibility and functionality in implementation and a very good compromise between area precision and performance over the other existing solutions.

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