A Simple Analysis to Determine the Limits of a CMOS Technology to Implement SC DC-DC Converters

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Abstract. This paper presents a simple analysis that allows to determine the maximum power density and efficiency of a SC DC-DC converter for a given CMOS technology. By determining the values of the ratio between the switches' gate capacitance and channel width, and between the ON resistance and the channel width, together with the parasitic capacitances from the flying capacitor, it is possible to plot the efficiency as a function of the power density for a given input voltage and output voltage of the converter, allowing to quickly determine both the expected efficiency of the converter and clock frequency ranges, for a given CMOS technology.

Keywords: power management unit, switched-capacitor (SC) converter, design techniques

1 Introduction

Nowadays, with the growing number of Internet-of-things (IoT) devices, the collection of real live raw data from innumerous processes has greatly increased, e.g., in industrial, health, transportation, communications processes and others [1]. This raw data can be analyzed inside of the IoT device thus distributing the data processing capabilities and decreasing the reaction time. This sensing and processing of information costs energy. Hence, it is extremely important to have efficient systems, in a macro scale it contributes for reducing the carbon footprint, and at a small scale, it allows improving the battery life of devices thus reducing maintenance costs.

There are several energy sources, like solar, piezoelectrical, thermal, and others [2]. This energy can be fed directly to the system, and/or be stored in an energy storing device, like a battery or supercapacitor. These energy sources produce a variable voltage, which requires the use of a Power Management Unit (PMU) to obtain a constant output voltage. The PMU provides a bridge between the energy sources and the system using, for example, DC-DC converters. These can be inductive or capacitive, where the latter has receiving a lot of attention in recent years since they are composed by switches and capacitors that are native in CMOS technology and thus, they can be easily integrated, resulting in a smaller footprint and cost, and still achieve high performance values [2]–[6].

The Switched-Capacitor (SC) DC-DC converters transfer charge from the input to the output through a capacitor, where the frequency at which the charge is transferred will determine the output voltage value of the converter. This charge transferring is controlled by a clock signal, allowing for different circuit configurations on each clock phase. The quality of both the capacitors and switches will affect the converter's energy efficiency and power per area value [6]–[8]. The characteristics of the passive devices depend on the CMOS technology node for the system implementation, for example, the lower the CMOS node, the higher the capacitance per area of the capacitors. This is because smaller oxide thickness means higher capacitance values. However, small oxide thickness also means lower breakdown voltage values and larger current leakage. The same goes for switches, the lower the node, the higher switching frequency can be. This raises the question, what is the expected performance for each technological node? To answer this, this work shows an analysis that characterizes both the capacitors and switches of the 130 nm bulk CMOS technology into a set of coefficients that are used to determine the converter efficiency and power per area. This can be applied to any technology node.

2 Relationship to Technological Innovation for Life Improvement

The IoT devices can enhance our life quality in many ways, e.g., increasing the surgery span of patient with medical embedded devices, like pacemakers, by increase the battery life of the devices. Such devices can also be used to monitoring our health, which can give us a better control of our daily life needs. There are several number of other examples in different areas, where all these devices, which need energy to operate, will benefit from energy efficient PMUs. The energy improvement of such devices will consequently have a direct impact on the human's life quality.

3 SC DC-DC Converter Theoretical Analysis

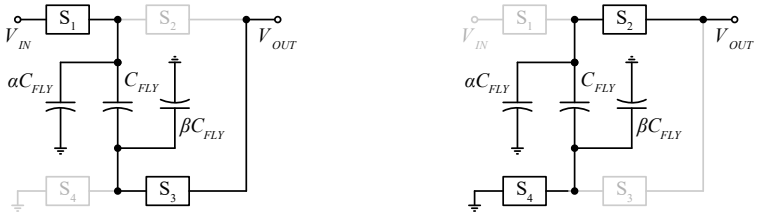
Fig. 1 shows the schematic of a Step-down Series-Parallel (SP) SC DC-DC converter with a Conversion Ratio (CR) of 1/2. It is composed by 1 flying capacitor C_{FLY} and 4 switches, where $S_{1,3}$ are ON in the phase ϕ_1 and $S_{2,4}$ are ON in phase ϕ_2, where $\phi_{1,2}$ are two clock signals complementary to each other. Hence, on ϕ_1, C_{FLY} connects between the input voltage V_{IN} and the output voltage V_{OUT}, and on ϕ_2, C_{FLY} connects between V_{OUT} and ground. In the schematic it is also represented the C_{FLY} parasitic capacitances by α and β, these refer to the top and bottom parasitic capacitance, respectively, as percentage of C_{FLY}. Assuming that V_{OUT} is kept at a constant voltage, the charge equations can be drawn:

$$(V_{IN} - V_{OUT})\, C_{FLY} + V_{IN}\, (\alpha\, C_{FLY}) = V_{OUT}\, (C_{FLY} + \alpha\, C_{FLY}) + \Delta q_o^{\phi_2}\,, \tag{1}$$

$$-V_{OUT}\, C_{FLY} = (V_{OUT} - V_{IN})\, C_{FLY} + V_{OUT}\, (\beta\, C_{FLY}) + \Delta q_o^{\phi_1}\,, \tag{2}$$

$$V_{OUT}\,(C_{FLY}+\alpha\,C_{FLY}) = (V_{IN}-V_{OUT})\,C_{FLY} + V_{IN}\,(\alpha\,C_{FLY}) - \Delta q_i^{\Phi_1}\ . \tag{3}$$

where $\Delta q_o^{\Phi_{1,2}}$ are the amount of charge absorbed by V_{OUT}, in the respective phase, and $\Delta q_i^{\Phi_1}$ the amount of charge drawn by the circuit from V_{IN}, in this case only during ϕ_1.



(a) Phase ϕ_1 **(b)** Phase ϕ_2

Fig. 1 Simplified schematic of the SP 1/2 SC DC-DC converter in each clock phase [3],[4].

These equations can be solved in respect to $\Delta q_i^{\Phi_1}$, $\Delta q_o^{\Phi_1}$, and $\Delta q_o^{\Phi_2}$, and used to determine the input and output current and power:

$$I_{IN} = \Delta q_i^{\phi_1}\,F_{CLK} = C_{FLY}\left(V_{IN}\,(1+\alpha) - V_{OUT}\,(2+\alpha)\right), \tag{4}$$

$$I_{OUT} = \left(\Delta q_o^{\phi_1} + \Delta q_o^{\phi_2}\right)F_{CLK} = C_{FLY}\,F_{CLK}\left(V_{IN}\,(2+\alpha) - V_{OUT}\,(4+\alpha+\beta)\right), \tag{5}$$

$$P_{IN} = V_{IN}\,I_{IN} = C_{FLY}\,F_{CLK}\,V_{IN}\left(V_{IN}\,(1+\alpha) - V_{OUT}\,(2+\alpha)\right), \tag{6}$$

$$P_{OUT} = V_{OUT}\,I_{OUT} = C_{FLY}\,F_{CLK}\,V_{OUT}\left(V_{IN}\,(2+\alpha) - V_{OUT}\,(4+\alpha+\beta)\right). \tag{7}$$

The converter efficiency η can be obtained by (8) and its output impedance R_{OUT} by (9). Both V_{OUT} and F_{CLK} can be determined by (10) and (11), where R_L is the load resistor and $P_{OUT} = V_{OUT}^2/R_L$.

$$\eta = \frac{P_{OUT}}{P_{IN}} = \frac{V_{OUT}\left(V_{IN}\,(2+\alpha) - V_{OUT}\,(4+\alpha+\beta)\right)}{V_{IN}\left(V_{IN}\,(1+\alpha) - V_{OUT}\,(2+\alpha)\right)}, \tag{8}$$

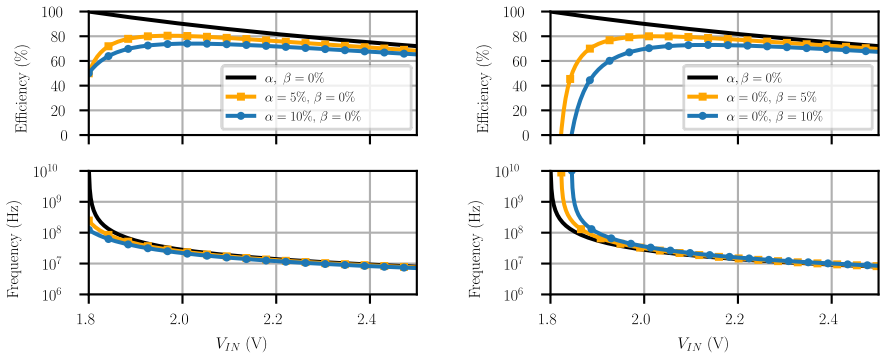
$$R_{OUT} = \frac{C R\,V_{IN} - V_{OUT}}{I_{OUT}} = \frac{V_{IN} - 2\,V_{OUT}}{2\,C_{FLY}\,F_{CLK}\left(V_{in}\,(2+\alpha) - V_{OUT}\,(4+\alpha+\beta)\right)} = \Big|_{\alpha,\beta=0} \frac{1}{4\,C_{FLY}\,F_{CLK}}, \tag{9}$$

$$V_{OUT} = I_{OUT} R_L \Rightarrow V_{OUT} = \frac{C_{FLY}\,F_{CLK}\,R_L\,V_{IN}\,(2+\alpha)}{1 + C_{FLY}\,F_{CLK}\,R_L\,(4+\alpha+\beta)}, \tag{10}$$

$$F_{CLK} = \frac{V_{OUT}}{C_{FLY}\,R_L\left(V_{IN}\,(2+\alpha) - V_{OUT}\,(4+\alpha+\beta)\right)} = \frac{P_{OUT}}{C_{FLY}\,V_{OUT}\left(V_{IN}\,(2+\alpha) - V_{OUT}\,(4+\alpha+\beta)\right)}. \tag{11}$$

Fig. 2 shows the converter's η and F_{CLK} as a function of V_{IN} for different values of α and β, with $C_{FLY} = 100$ pF, and $P_{out} = 1$ mW. The graphs show that while both parasitic capacitances have a negative impact on both η and F_{CLK}, the top parasitic capacitance has a smaller impact when compared to the bottom parasitic capacitance. Moreover, it pushes the peak efficiency for lower V_{IN} values while decreasing F_{CLK} for the same input/output ratio. This is because the charge absorbed on ϕ_1 is supplied to V_{OUT} on ϕ_2. This acts like a parallel 1/1 converter and thus allowing the converter to work at a lower F_{CLK} value for the same input/output voltage ratio. Hence, in this

topology, when implementing the C_{FLY} the highest parasitic plate should be connected as the top parasitic capacitance [9]. These equations were validated through electrical simulations in [10], [11].



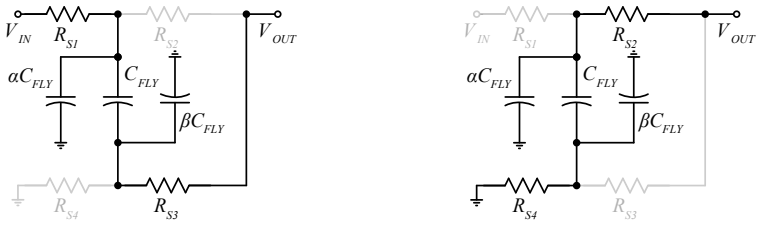
(a) Top parasitic capacitance ($\beta = 0\%$). **(b)** Bottom parasitic capacitance ($\alpha = 0\%$).

Fig. 2 Efficiency as a function of $\boldsymbol{V_{IN}}$, for $\boldsymbol{V_{OUT} = 0.9}$ V, $\boldsymbol{C_{FLY} = 100}$ pF, and $\boldsymbol{P_{out} = 1}$ mW.

Expression (8) assumes that the clock phases are long enough to allow C_{FLY} to completely charge (or discharge), however, the finite R_{ON} value of the switches cause partial charging depending on F_{CLK}, hence it will have an impact on the converter efficiency [5]. According to [5], R_{OUT} can be re-written to take in the effect of partial charging:

$$R_{OUT} = \frac{1}{\gamma} \frac{1}{4\, C_{FLY}\, F_{CLK}}, \tag{12}$$

this equation is identical to (9) except for a scaling factor, γ, which accounts for incomplete charging [5]. Let τ' be everything else that is in the exponential before F_{CLK} ($\tau' = 2\, R_{ON_{tot}}\, C_{FLY}$), then the number of time constant in a period sets the value of γ. For $3\tau'$, the γ value is 90.05%, for $4\tau'$, it is 96.40%, and for $5\tau'$ it is 98.66%. Thus, for values lower than $4\tau'$, the value of γ drops significantly. Hence, $4\tau'$ offers a good compromise point for sizing the converter switches without having a significant impact on the converter's efficiency. The $4\tau'$ allows to size the switches R_{ON} and thus determining the transistor's W. This allows to determine the power required to charge the gate switches' parasitic capacitance (C_{GG}), which will also impact the converter's efficiency.



(a) ϕ_1. **(b)** ϕ_2.

Fig. 3 Simplified schematic of the converter with the switches replaced by R_{ON}.

Fig. 3 shows the converter's schematic with its ON switches replaced by the respective R_{ON}. Both ϕ_1 and ϕ_2 have the same time constant given by:

$$\tau = R_{ON_{tot}} C_{FLY} = \frac{1}{2F_{CLK}}\,, \tag{13}$$

where $R_{ON_{tot}} = R_{ON_{S1}} + R_{ON_{S2}}$ is the total resistance value of switches in series per phase. Assuming that $R_{ON_{S1}} = R_{ON_{S2}} = R_{ON}$ which means that $R_{ON} = R_{ON_{tot}}/2$, then, the R_{ON} value for the $4\tau'$ operation point is given by

$$R_{ON_{total}} = \frac{1}{4\tau'} = \frac{1}{8\,C_{FLY}\,F_{CLK}} \Rightarrow R_{ON} = \frac{1}{16\,C_{FLY}\,F_{CLK}}\,. \tag{14}$$

For small drain-to-source voltages ($V_{DS} \ll V_{GS} - V_{TH}$), the switch R_{ON} and C_{GG} are given by:

$$R_{ON} \cong \frac{L}{C_{ox}\mu_n W(V_{GS}-V_{TH})} \approx \frac{k_R}{W}\,, \tag{15}$$

$$C_{GG} = C_{GD} + C_{GS} \cong WLC_{ox} + WC_{ov} \approx k_C W\,. \tag{16}$$

These equations show that R_{ON} is inversely proportional to the transistor's width (W), and that C_{GG} is directly proportional to W. Furthermore, if V_{GS}, L, C_{ox} and μ_n are kept constant, and $V_{DS} \ll V_{GS} - V_{TH}$, then the previous equations can be approximated by a constant coefficient, k_R and k_C, that relates both R_{ON} and C_{GG} with W [10], [12]. Hence, C_{GG} can be given by (17). The switches' power dissipation can be determined by summing all the switches' C_{GG} and multiplying it by F_{CLK} and the switches drive voltage V_{SW} squared, as shown in equation (19). Notice that P_{SW} is given by the sum of the k_R and k_C coefficients of each switch, where N is the total number of switches, where $K_{SW} = k_{C_1}\,k_{R_1} + k_{C_2}\,k_{R_2} + \cdots + k_{C_N}\,k_{R_N}$.

$$C_{GG} = \frac{K_R\,K_C}{R_{ON}} = 16\,k_C\,k_R\,C_{FLY}\,F_{CLK}\,, \tag{17}$$

$$P_{SW} = \left(C_{GG_{S1}} + C_{GG_{S2}} + C_{GG_{S3}} + C_{GG_{S4}}\right) F_{CLK}\,V_{SW}^2 = \tag{18}$$

$$= 16\left(k_{C_1}\,k_{R_1} + \cdots + k_{C_N}\,k_{R_N}\right) C_{FLY}\,F_{CLK}^2\,V_{SW}^2 = 16\,K_{SW}\,C_{FLY}\,F_{CLK}^2\,V_{SW}^2\,. \tag{19}$$

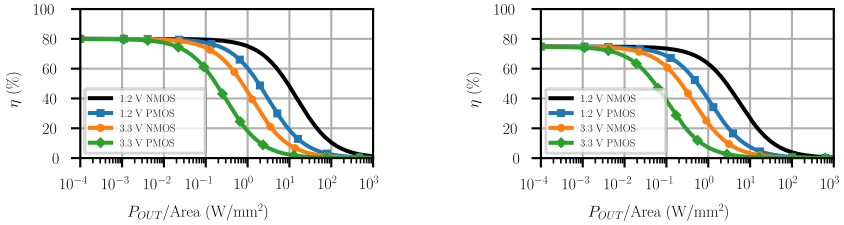
The effect of P_{SW} can now be added to the converter's efficiency, resulting in

$$\eta = \frac{P_{OUT}}{P_{IN}+P_{SW}} = \frac{V_{OUT}\left(V_{IN}\,(\alpha+2) - V_{OUT}\,(\alpha+\beta+4)\right)}{16\,F_{CLK}\,V_{OUT}^2\,K_{SW} + V_{IN}^2\,(\alpha+1) - V_{IN}\,V_{OUT}\,(\alpha+2)}\,. \tag{20}$$

Due to the F_{CLK}^2 in (19), F_{CLK} does not cancel out in (20). Thus, replacing F_{CLK} by (11) and considering that C_{FLY} can be given by the the capacitance area A_c times C_{den} of the device chosen to implement it, e.g. 10 fF/μm^2 in the MOS capacitor. Then, C_{FLY} can be re-written by $C_{FLY} = A_c \times C_{den}$. This gives η as a function of P_{OUT} per capacitance area, i.e. power density, as shown below.

$$\eta = \frac{V_{OUT}\left(V_{IN}\,(\alpha+2)-V_{OUT}\,(\alpha+\beta+4)\right)}{V_{IN}^{2}\,(\alpha+1)-V_{IN}\,V_{OUT}\,(\alpha+2)+\frac{16\,K_{SW}\,P_{OUT}\,V_{OUT}}{A_c\,C_{den}\left(V_{IN}\,(2+\alpha)-V_{OUT}\,(4+\alpha+\beta)\right)}}. \tag{21}$$

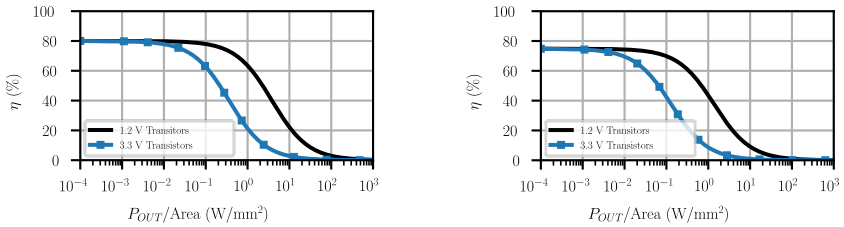
The equation above allows to determine the converter's efficiency as a function of the power density for a given V_{IN} and V_{OUT}, and for a given K_{SW}, which depends on the type of transistors chosen to implement the switches. Considering four different cases, where the transistors are all implemented by 1.2 V ($k_R = 577.40\ \Omega\cdot\mu m^2$ and $k_C = 1.34\ fF/\mu m^2$) and 3.3 V ($k_R = 5337.56\ \Omega\cdot\mu m^2$ and $k_C = 1.77\ fF/\mu m^2$) NMOS transistors, 1.2 V ($k_R = 2709.51\ \Omega\cdot\mu m^2$ and $k_C = 1.41\ fF/\mu m^2$) and 3.3 V ($k_R = 20570.40\ \Omega\cdot\mu m^2$ and $k_C = 1.95\ fF/\mu m^2$) PMOS transistors, the k_R and k_C were taken for a $V_{GS} = 0.9$ V through electrical simulations. Fig. 4 (a) and (b) show the efficiency (21) as a function of the power density for $V_{SW} = V_{OUT} = 0.9$ V and for C_{FLY} implemented by a PMOS transistor ($C_{den} = 10\ fF/\mu m^2$, $\alpha = 4.5\ \%$, and $\beta \approx 0\ \%$). As expected, the graph clearly show that 1.2 V transistors are preferable in comparison with 3.3 V transistors. Furthermore, 1.2 V NMOS transistors allow maximizing the efficiency and power density. However, 1.2 V transistors may not be an option if their voltages exceed the transistor's breakdown voltage. Moreover, 1.2 V NMOS requires $V_{GS} > V_{th}$, which in the case switch S_1 it would require a gate voltage higher than V_{IN}. Hence, choosing to implement S_1 with a 1.2 V PMOS transistor can be a good compromise given the complexity of the NMOS driver would require.



(a) $V_{IN} = 1.9$ V **(b)** $V_{IN} = 1.85$ V

Fig. 4 Converter's $\boldsymbol{\eta}$ as a function of $\boldsymbol{P_{OUT}/A_c}$ for different switches' implementation with $\boldsymbol{V_{OUT} = 0.9}$ V.

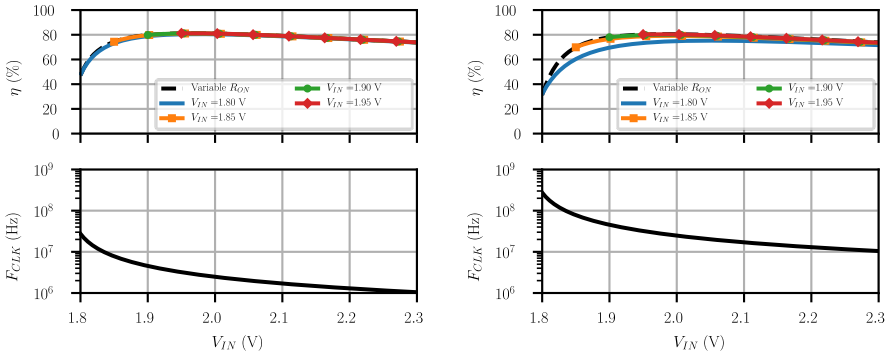
Fig. 5 (a) and (b) show the efficiency (21) as a function of the power density with $S_{1,2,3}$ implemented with PMOS transistors and S_4 with an NMOS transistor, C_{FLY} implemented with a PMOS transistor, and for $V_{OUT} = 0.9$ V. The graphs show that depending on the input voltage limit, the maximum power density, whilst keeping efficiency constant, is within the 10 to 100 mW/mm², depending if either 1.2 V or 3.3 V transistors are used.



(a) $V_{IN} = 1.9$ V **(b)** $V_{IN} = 1.85$ V

Fig. 5 Converter's $\boldsymbol{\eta}$ as a function of $\boldsymbol{P_{OUT}//A_c}$ with $\boldsymbol{S_{1,2,4}}$ implemented with PMOS transistor and $\boldsymbol{S_3}$ with NMOS transistor, for $\boldsymbol{V_{OUT} = 0.9}$ V.

It is important to notice that once the switch is sized, the switches' R_{ON} is fixed throughout the whole V_{IN} range. In the previous graphs, the switch's R_{ON} was modified according to the V_{IN} value. In a real scenario, the converter's minimum V_{IN} value must be fixed, which sets the minimum R_{ON} value. Hence, the previous analysis is used to set $R_{ON_{Min}}$ and then η is recalculated using the constant $R_{ON_{Min}}$ value throughout the whole V_{IN} range.



(a) 10 mW/mm^2. **(b)** 100 mW/mm^2

Fig. 6 Converter's $\boldsymbol{\eta}$ with both the $\boldsymbol{C_{FLY}}$ and the switches' parasitic capacitances for a fixed $\boldsymbol{R_{ON}}$ value determined by the minimum $\boldsymbol{V_{IN}}$ value of the converter, for $\boldsymbol{V_{OUT} = 0.9}$ V.

Fig. 6 (a) and (b) show η recalculated using the R_{ON} calculated for different V_{IN}, for 10 mW/mm^2 and 100 mW/mm^2. The efficiency values after $V_{IN_{limit}}$ are not drawn because F_{CLK} increases beyond the $4\tau'$ limit resulting in incomplete settling, making the equation no longer valid. These graphs show that as $V_{IN_{limit}}$ gets closer to the voltage CR there is a significantly impact on η, especially at high power density values, such as 100 mW/mm^2. Hence, avoiding working close to the CR voltage value (1.8) is recommend because the value of R_{ON} is extremely low. Furthermore, the frequency increases rapidly close to the CR voltage value, hence any deviation from that point would cause V_{OUT} to rapidly deviate from the 0.9 V target. Nonetheless, the previous analysis with the variable R_{ON} and with fixed R_{ON} are quite similar when working under the maximum power density (<100 mW/mm^2) and far enough from the CR voltage value ($V_{IN} > 1.85$). The efficiency plot should be analyzed together with F_{CLK} because, as Fig. 6 (b) shows, to achieve a power density of 100 mW/mm^2 the converter must work at frequencies of 10 to 100 MHz, which adds complexity to the system design, mainly the clock generator and the switch drivers. Hence lower power densities, such has the ones in Fig. 6 (a) may be preferable, due to the lower F_{CLK} value.

4 Conclusions

This paper describes a theorical analysis that allows characterizing the performance of an SC DC-DC converter for a given technological node. In this case, the 130 nm CMOS technology was chosen to implement a 1/2 SP SC DC-DC converter for converting an input voltage range of 2.3 to 1.8 V to an output voltage of 0.9 V. The results show that with this topology and technology the maximum efficiency would be around 80% and the power density per area in the range of 10 to 100 mW/mm^2, depending on the transistors chosen to implement the passive devices.

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