A Multi-DSP 96002 board

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Chapter 1

MD96-TECHNICAL MANUAL

1.1 Introduction

MD96 is the name of the Multi-DSP 96002 board developed in Robotvis department (INRIA-Sophia), during ESPRIT P940 European project, in 1989.

The MD96 is a high integrated board, using four Motorola 96002 Digital Signal Processors and interfaced with the VMEbus.

This document is a general overview of the MD96, its synoptic, its performance and its installation guide, with also an overview of the processor used.

Two other chapters are about the MD96. A Hardware Annexes explains in details how the MD96 works, it includes the schematics and the PLDs equations. A Software support gives the C functions syntax of the MD96 library. These functions allows you to develop application on the MD96, it includes functions to connect the MD96 and the Host machine (SUN, VxWorks system, ...) and functions which are internal functions of the MD96 (inter DSP communication, VMEbus accesses, DMA transfer, ...).

This chapter consists of four parts :

- The first one provides a general view of the board. It explains the global architecture of the MD96, then a general view of the processor, and some information about its implementation are given.
- The second one gives a full description of the board, and explains the different element build around the data path on the MD96.
- The installation guide allows to insert the MD96 in a VMEbus system. Some figures about electrical consumption, mechanical, and data transfer timing specifications are also given.
- The fourth part gives generalities about System Integration, Communication, and about future expansion for the MD96.

The architecture of the MD96 allows a great reduction in terms of time computation in regard to a workstation, if they fit these requirements :

- Firstly, application must use the maximum of the DSP 96002 features. That means, to have a great amount of floating point operations, to use trigonometry (Look Up Table in the DSP 96002) or to accept perfectly DSP 96002 memory mapping (X,Y,P fields).
- Secondly, it must use the MD96 features. That means to be parallelized in a small number of tasks (between 4 and 16), to use the inter-DSP communication, not to be too greedy in terms of memory space (Only 9 Megabytes are available).

1.2 MD96 Overview

The MD96 is VMEbus interfaced board achieving a peak processing power of 240 MFLOPS.

The main features of the MD96 are :

- Four Processing Elements (PE), working in parallel. Each PE is composed of a 96002 Digital Signal Processor at 33 or 40 MHz and one or two JEDEC memory modules. The memory modules are organized in 64Kx32, 128Kx32 or 256Kx32. Thus, each DSP can have 2 Mbytes of fast static memory.
- A On Board Shared bus between the four PE, the VMEbus and a Common memory (64 Kwords to 256 Kwords). This Common memory is one JEDEC module of 64Kx32 up to 256Kx32. This Common bus allows PE to create fast communication channels between them and to share data using a Common memory. This memory could also be used by the VMEbus interface.
- Each PE can be master or slave on the VMEbus allowing the board to work without any master board. (except for boot operation). The VMEbus interface module is fully compliant with the VMEbus specification (Revision C.1). The interface is a module which is A32-D32 MASTER/SLAVE (allowing 32-bit data transfers), A24-D32 MASTER/SLAVE and A24-D16 MASTER.
- The Arbiter, Interrupter and Timer modules of the VMEbus specification are not provided on the DSP board.
- A Broadcast transfer can take place on the VMEbus to simultaneously access several MD96. It allows a simultaneous write into the Common memory. Because Broadcast transfer is not support by VMEbus, two external rows of the P2 connector are used to provide this feature.
- Remote Reset facility for each PE is provided.
- Interrupt generation facilities : The VMEbus interface is able to generate VMEbus interrupts with programming interrupt levels and vectors. This function is used by the PE to provide synchronism with the supervisor and is very efficient for real time application.
- Each PE module can be interrupted by VMEbus. In fact you can activate three different interruptions by DSP.
- A DSP OnCE (MOTOROLA Trademark) debug interface will be implemented on the MD96 to debug the DSPs. This interface is mapped into the VMEbus world register mapping able to access the serial OnCE DSP interface. This interface will be used later for high level debugging.
- There is no need for a bootstrap memory EPROM on the board, since each DSP will be start up from its Host interface. This feature saves four EPROM devices, but requires a Host intervention at RESET. It allows a complete reconfiguration of the board, both for the user program and the development tools.
- The MD96 is constituted of standard CMOS/TTL components only, and is implemented on a extended double Euro-Card (220 mm x 233 mm).

The MD96 accepts up to 9 Mega Bytes of fast access memory, which is useful to support C applications. It efficiently uses the dual port DSP capability. Each DSP can work in its Local memory (port B) with zero Wait State and no bus arbitration, and the Common bus (port A) can be used by each DSP with one Wait State, or by the VMEbus with a minimum of arbitration. (fig 1 summarize the MD96 hardware architecture).