

The Non-Smooth Approach applied to simulating Integrated Circuits and Power Electronics Evolution of electronic circuit simulators towards fast-SPICE performance

Pascal Denoyelle, Vincent Acary

▶ **To cite this version:**

Pascal Denoyelle, Vincent Acary. The Non-Smooth Approach applied to simulating Integrated Circuits and Power Electronics Evolution of electronic circuit simulators towards fast-SPICE performance. [Technical Report] 2006. inria-00080839v1

HAL Id: inria-00080839

https://inria.hal.science/inria-00080839v1

Submitted on 20 Jun 2006 (v1), last revised 21 Jun 2006 (v2)

HAL is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.

INRIA

INSTITUT NATIONAL DE RECHERCHE EN INFORMATIQUE ET EN AUTOMATIQUE

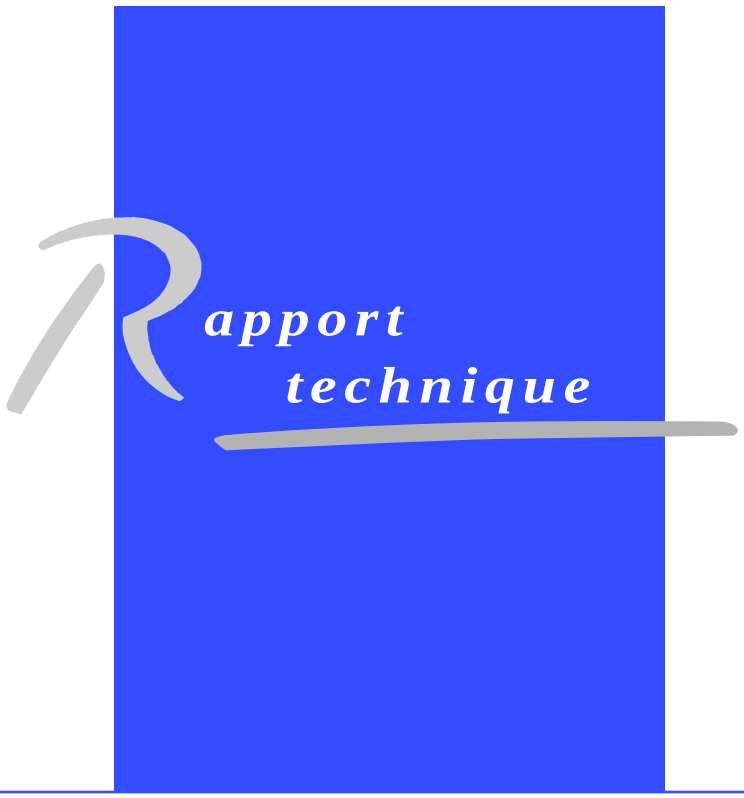
The Non-Smooth Approach applied to simulating Integrated Circuits and Power Electronics Evolution of electronic circuit simulators towards fast-SPICE performance

Pascal Denoyelle — Vincent Acary

N° ????

20 Juin 2006

Thème NUM



ISSN 0249-0803 ISRN INRIA/RT--????--FR+ENG

The Non-Smooth Approach applied to simulating Integrated Circuits and Power Electronics Evolution of electronic circuit simulators towards fast-SPICE performance

Pascal Denoyelle * , Vincent Acary †

Thème NUM — Systèmes numériques
Projet BIPOP

Rapport technique n° ???? — 20 Juin 2006 — 45 pages

Abstract: Numerical simulation is a key element in the design of electronic circuits. Huge efforts were devoted to it in the past 30 years allowing to fully benefit from the possibilities provided by circuits and components fabrication technologies.

A threshold in the shrinking of components was exceeded these last years. Besides the positive effect on the integration of functions into a single chip and on the elementary power consumption, negative effects appear as electrical parasitic phenomena previously neglected. Simulations are therefore much longer despite the increased performances of computers because elementary components models are more complex and the components count increases.

In this report, we present an history of the models and algorithms that are classically used to simulate a circuit at the electrical level. Thereafter, we introduce the so-called non-smooth class of models and algorithms studied at the INRIA, as well as the first results that they yielded in the simulation of simple circuits. The non-smooth approach seems to be a promising solution for the large scale electrical simulation.

Key-words: electronic circuit, nanotechnologies, numerical simulation, non-smooth system, LCP

Version 1, Juin 2006

* Pascal.Denoyelle@inria.fr
† Vincent.Acary@inria.fr

Unité de recherche INRIA Rhône-Alpes
655, avenue de l'Europe, 38334 Montbonnot Saint Ismier (France)
Téléphone : +33 4 76 61 52 00 — Télécopie +33 4 76 61 52 52

L'approche non-régulière appliquée à la simulation des circuits intégrés et de l'électronique de puissance Evolution des simulateurs de circuits électroniques vers un mode SPICE rapide

Résumé : La simulation numérique est un des éléments-clés dans la conception des circuits électroniques. Les efforts importants qui y sont consacrés depuis 30 ans ont jusqu'ici permis de tirer pleinement parti des possibilités offertes par les technologies de fabrication des circuits et composants.

Ces dernières années, un seuil a été franchi dans la miniaturisation. Outre l'effet positif sur l'intégration des fonctions dans un circuit unique et sur les consommations élémentaires, des effets négatifs apparaissent comme la manifestation de phénomènes électriques parasites autrefois négligés. Les simulations sont ainsi beaucoup plus longues en dépit des meilleures performances des ordinateurs car les modèles de composants élémentaires se complexifient et le nombre de ces composants s'accroit.

Nous présentons dans ce rapport un historique des modèles et des algorithmes classiquement utilisés pour simuler un circuit au niveau électrique. Ensuite, nous abordons la classe de modèles et d'algorithmes dits non-réguliers étudiés à l'INRIA et les premiers résultats de simulation de circuits élémentaires qu'ils ont permis d'obtenir. L'approche non-régulière apparait comme une solution prometteuse pour la simulation électrique à grande échelle.

Mots-clés : circuit électronique, nanotechnologies, simulation numérique, système non-régulier, LCP

Contents

1 Introduction **5**

2 State-of-the-art time domain electrical simulators **7**
2.1 Electrical models 7
2.2 Methods for setting up the equations 9
2.2.1 The Sparse Tableau Approach (STA) 9
2.2.2 The Modified Nodal Analysis (MNA) 11
2.3 Numerical algorithms 12
2.3.1 Solving the DC problem 13
2.3.2 Numerical integration of differential algebraic equations 16

3 Recent approaches to the fast simulation of large circuits **17**

4 The non-smooth approach **21**
4.1 The mathematical framework of the non-smooth approach 21
4.2 Simulation results and comparisons:power electronics 23
4.2.1 The example of the RLCD circuit 23
4.2.2 Diodes bridge circuit simulation 26
4.2.3 Power converters 26
4.3 Simulation results and comparisons:MOS transistors and inverters 32
4.3.1 Piecewise linear model of a MOS transistor 32
4.3.2 Inverter chain 36

5 Conclusion **41**

Chapter 1

Introduction

Electronic circuits - either integrated on a single substrate or as a set of components on a board - are very often a complex assembly of a lot of basic components with non linear characteristics.

Designers of electronic products are relying on various checking softwares among which electrical time domain simulators were the first to be developed in the early 1970s. The SPICE 2 simulator (Simulation Program with Integrated Circuit Emphasis) was released in 1975 by the Berkeley university as a free software. It allows to have insight into the evolution of voltages and currents in a circuit modelled as an assembly of dipoles. Some of the algorithms embedded in SPICE evolved in commercial versions, but the main original features were kept: use of smooth models and solving a set of non linear equations with Newton-Raphson algorithm or its variants. The models of devices and especially of MOS transistors followed the increasing role of parasitic effects due to geometries shrinkage and speed's increase.

Besides this 30 years story, electronics circuits evolved:

the Integrated Circuits (IC) technologies now allow to integrate hundreds of millions of transistors switching at GHz frequencies on a die of $1\,cm^2$. It is out of question to simulate a whole such IC with a SPICE simulator, even with today's computers ! Thus developers mainly rely on a thorough SPICE simulation of small subsets of circuits (logic gates) providing a coarse model of each subset that will be used in a less accurate simulator (logic simulator).

Nevertheless, some parasitic effects that can strongly affect the operation (crosstalk between lines, signal integrity, power distribution) have to be carefully considered. Some of these even require a physical model to be properly characterized (i.e a surface or volume model yielding a set of partial differential equations). With an electrical simulator like SPICE, it is still possible to study their effects. But a logic simulator used for a whole chip simulation cannot handle properly these effects. Thus there is

today a need for a fast time domain electrical simulator that will allow their simulation with an accuracy as close as possible to SPICE, and much faster.

Mixed-signal circuits and power electronics: these circuits involve interacting analog and digital parts. Due to the complexity of the digital part, a SPICE simulation of the whole is often too long. Thus people have to use simulators with two kernels: one event-driven and finite-state values kernel for the digital part and a time-step, real values kernel solving differential equations for the analog part. The link between both kernels relies on a set of rules to provide synchronization between them. The accuracy of results can be impaired by the more abstract modeling of the logic part and to errors linked to the synchronization rules. Thus a fast time domain simulator is also required to properly analyze this kind of circuit.

In this report, we will first review the basic principles of the state-of-the-art time domain simulators, and summarize the features of the latest commercial simulators called "fast SPICE". Then we will describe the non-smooth approach in modelling and simulating dynamical systems, a research field of the BIPOP team at INRIA Rhône-Alpes. We will see that this approach already yields interesting results when it is applied to electronics, and that it could become an alternate to state-of-the-art simulators, enabling the analysis of a larger number of elementary devices.

Chapter 2

State-of-the-art time domain electrical simulators

The SPICE simulator ([Nag75]) is based on the following models and solvers.

2.1 Electrical models

An electrical model of a circuit is based on an assembly of elementary components (voltage or current source, resistor, capacitor, transistor...). The connection points are called *poles*. Unlike physical models that involve a thorough set of complex partial differential equations, electrical models aim at describing the response of a device through:

- a small number of variables (poles potentials and branch currents)
- a "reasonable" number of parameters
- a differential algebraic equation associated with the static and dynamic characteristics linking these variables and parameters

For instance, the electrical model of a diode is a 3 dipoles assembly as shown in Figure 2.1. Except for the resistor, the other parts (voltage-controlled current source and voltage-controlled capacitor) imply a nonlinear characteristic. The static characteristic $I(V)$ of the current source is described by Shockley's law:

$$I = I_S.(e^{\frac{q.V}{N.k.T}} - 1) \qquad \text{when} \quad V > -5.N.\frac{k.T}{q}$$

$$I = -I_S \qquad \text{when} \quad V < -5.N.\frac{k.T}{q}$$

with

V , I	voltage across the source and current through the source
I_S	saturation current, default value 10^{-14} A
q	electron charge $1.6\,10^{-19}$ C
k	Boltzmann constant $1.38\,10^{-23}\,J.K^{-1}$
T	temperature in K
N	emission coefficient

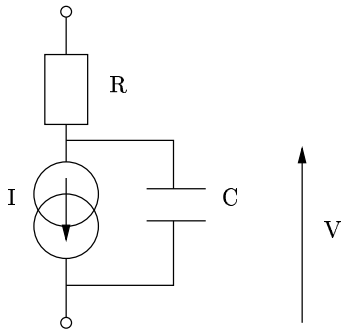


Figure 2.1: Electrical model of a diode

Transistors are also modelled as an assembly of sources, resistors, capacitors with non linear characteristics. At the end, the electrical model of a whole circuit is thus a large assembly of elementary dipoles.

Despite the relative simplicity of electrical models compared to physical models, modelling specialists try to provide a good accuracy even when complex mechanisms have to be taken into account. This is why the electrical models of MOS transistors involve now tens of parameters. The increasing number of parameters is not only a matter of 3^{rd} or 4^{th} order accuracy: it reflects the increasing part of effects that used to be considered as parasitics but that now have 1^{st} order values.

Remark 1 *The state-of-the-art electrical models are based on explicit formulae with requirements on the existence of derivatives: at least output variables should be one time derivable with respect to each input to allow the solving of equations by the state-of-the-art simulators (see 2.2). Until the end of 1990's, the widely used models of MOS transistors were based on a function $I_{DS} = f(V_{GS}, V_{DS})$ where f was defined by region of the V_{GS}, V_{DS} plane, and one time derivable. When simulations required a higher than one order of derivation, smoothing functions were introduced (BSIM3V3 model from Berkeley university, MM9 model from Philips) in a somehow artificial way. The most recent models (SP2001, MM11, EKV2.6) have also a high order differentiability, either resulting from a physical approach (SP2001, EKV2.6) or from smoothing functions (MM11).*

We will see later that the non-smooth approach enables to perform simulation with non-derivable and even non-continuous or multivalued functions.

2.2 Methods for setting up the equations

The inputs of a simulator consist basically of:

- a library file containing parameters for basic components provided by a semiconductor foundry or designer
- a netlist of components built possibly in a hierarchical way by instantiation of smaller netlists

From these inputs, the simulator identifies the set of unknowns to be computed at each time step and sometimes partitions them into subsets to apply a block-based algorithm. During the simulation, matrices are assembled to transform the analytic formulation of differential algebraic equations into a set of linear equations. Except in the (rare) case of a linear constant circuit, matrix assembly is done several times per time step.

We will now review the main approaches to this matrix assembly: the Sparse Tableau Approach and the Modified Nodal Analysis. The underlying theory will be explained thanks to the example of a circuit consisting of an LC oscillator supplying a load resistor through a half-wave rectifier (see Figure 2.2).

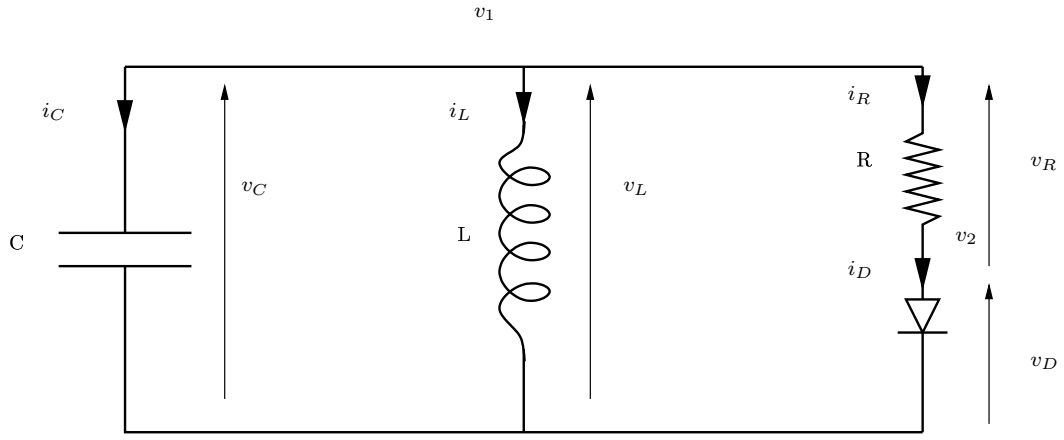


Figure 2.2: Electrical oscillator with half-wave rectifier

2.2.1 The Sparse Tableau Approach (STA)

In this method ([HBG71]), the variables are:

- all node potentials with respect to a common reference
- all branch voltages

- all branch currents

In a more general formulation, one can also use electric charge and magnetic flux instead of current or voltage for some components (e.g capacitor, inductor).

The equations are based on:

- Kirchhoff's voltage law that simply relates branch voltages to connected nodes potentials
- Kirchhoff's current law stating that the sum of currents of all branches converging to a node is zero
- the branch constitutive equations that model the behavior of components

We obtain then the following equation for the example of Figure 2.2:

v_C	capacitor voltage
i_C	capacitor current
v_L	inductor voltage
i_L	inductor current
v_R	resistor voltage
i_R	resistor current
v_D	diode voltage
i_D	diode current
v_1	node 1 potential
v_2	node 2 potential

Kirchhoff's voltage law is written:

$$\begin{aligned} v_C - v_1 &= 0 \\ v_L - v_1 &= 0 \\ v_R - v_1 + v_2 &= 0 \\ v_D - v_2 &= 0 \end{aligned}$$

Kirchhoff's current law is written:

$$\begin{aligned} i_C + i_L + i_R &= 0 \\ i_R - i_D &= 0 \end{aligned}$$

and the branch constitutive equations follow:

$$\begin{aligned} Cv'_C - i_C &= 0 \\ Li'_L - v_L &= 0 \\ v_R - Ri_R &= 0 \\ i_D - f(v_D) &= 0 \end{aligned}$$

where f is an exponential (Shockley's law). The dynamic behavior of the diode is neglected.

With an extended matrix formulation (to handle nonlinearity of the diode), one gets:

$$\begin{pmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ C & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & L & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \end{pmatrix} \cdot \begin{pmatrix} v'_C \\ i'_C \\ v'_L \\ i'_L \\ v'_R \\ i'_R \\ v'_D \\ i'_D \\ v'_1 \\ v'_2 \end{pmatrix}$$

$$+ \begin{pmatrix} 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & -1 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & -1 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & -1 & 1 \\ 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & -1 \\ 0 & 1 & 0 & 1 & 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 & 0 & -1 & 0 & 0 \\ 0 & -1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & -1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & -R & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 \end{pmatrix} \cdot \begin{pmatrix} v_C \\ i_C \\ v_L \\ i_L \\ v_R \\ i_R \\ v_D \\ i_D \\ v_1 \\ v_2 \end{pmatrix} + \begin{pmatrix} 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ -f(v_D) \end{pmatrix} = 0$$

thus a differential algebraic equation with sparse matrices and a nonlinear term. This method uses a lot of unknowns, resulting in the large size and sparsity of the matrices. Even if it is very general and allows a straightforward setting of equations, another method dealing with much less unknowns was preferred for the state-of-the-art simulator SPICE: the Modified Nodal Analysis.

2.2.2 The Modified Nodal Analysis (MNA)

The first version of nodal analysis considered only node potentials as unknowns and set the equations by:

- for each branch, the constitutive equation of the dipole is written in the form $i = Y \cdot (V_1 - V_2)$
- for each node, the Kirchhoff's current law is applied: $\sum i = 0$

yielding then an equation of the form $I = Y \cdot V$ with I a vector of 0 or current sources values, V a vector of unknown node potentials and Y the admittance matrix.

The nodal analysis had a serious drawback: it was assumed that the current is given explicitly in each branch by a source term or by a relation of the type $i = f(U, U')$. So inductors, voltage sources and several other standard electrical models could not be used.

For these reasons, it was modified ([HRB75]) by basically adding in the vector of unknowns some branch currents (for instance, the voltage source or inductor currents) and adding in the vector of data some known voltages. The MNA is widely used since it is the method that was chosen for the SPICE simulator developed at Berkeley University in the 1960's and 1970's, and that remains the standard for time domain analysis of circuits.

We will consider now how the circuit 2.2 is set into equations with the MNA. The unknowns are:

v_1 node 1 potential
v_2 node 2 potential
i_L inductor current

Two equations come from the Kirchhoff current law written at nodes 1 and 2, and the third equation is related to the inductor branch constitutive equation. We get then:

$$\begin{pmatrix} C & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & L \end{pmatrix} \cdot \begin{pmatrix} v_1' \\ v_2' \\ i_L' \end{pmatrix} + \begin{pmatrix} \frac{1}{R} & -\frac{1}{R} & 1 \\ \frac{1}{R} & -\frac{1}{R} & 0 \\ -1 & 0 & 0 \end{pmatrix} \cdot \begin{pmatrix} v_1 \\ v_2 \\ i_L \end{pmatrix} + \begin{pmatrix} 0 \\ -f(v_2) \\ 0 \end{pmatrix} = 0$$

thus a much more compact form than with the STA method.

2.3 Numerical algorithms

In the previous sections, we saw how to set up the equations in an analytic form. Thanks to the smooth nature of the models, the equations are differential algebraic equations (DAE) with most of the time nonlinear parts (like the diode $I(V)$ characteristic),

$$f(x', x, t) = 0$$

which can be often written in the form:

$$A \cdot x' + g(x) = S(t) \qquad \text{with } A \text{ a matrix and } S(t) = \text{independent sources}$$

If A is singular, which is the case with our example set up with the MNA, we have a DAE. If all unknowns derivatives are used (A invertible), we get an ODE (Ordinary Differential Equation).

The causality principle implies that we deal with an initial value problem: it is necessary to provide a consistent initial value for all unknowns of the DAE. This value may be obtained by an estimation, by sampling a previous simulation at a given instant, or, most of the time, it is computed as an equilibrium point (called DC) considering that all derivatives are initially zero and that source terms will later provide the dynamics.

We present here the numerical solutions used to solve the DAE. First of all, we will consider how to solve the DC (i.e constant values) problem, and see later how the transient analysis (time varying values) is handled.

2.3.1 Solving the DC problem

The DC problem is simplified to the equation $f(0, x, 0) = 0$ with f being most of the time a nonlinear function $\mathbb{R}^n \longrightarrow \mathbb{R}^n$. Mainly two approaches have been used in state-of-the-art simulators to solve it: the Newton-Raphson algorithm applied to the whole set of equations, and a relaxation method solving each equation one after the other.

The Newton-Raphson algorithm

This classical iterative method finds the zero (supposed to be existing and unique) of a continuously derivable function $f : \mathbb{R}^n \longrightarrow \mathbb{R}^n$ by:

1. Start with an initial guess x^0
2. Compute the Jacobian of f at estimate x^k :

$$J_f(x^k) = \begin{pmatrix} \frac{\partial f_1}{\partial x_1}(x^k) & \cdots & \frac{\partial f_1}{\partial x_n}(x^k) \\ \vdots & \ddots & \vdots \\ \frac{\partial f_n}{\partial x_1}(x^k) & \cdots & \frac{\partial f_n}{\partial x_n}(x^k) \end{pmatrix}$$

3. Compute a new estimate:

$$x^{k+1} = x^k - J_f(x^k)^{-1} \cdot f(x^k)$$

4. Compute $\|x^{k+1} - x^k\|_\infty = max_{i=1\cdots n}(|x_i^{k+1} - x_i^k|)$ and check for absolute or relative convergence by comparison with given thresholds. To avoid a false convergence, it is also necessary to check for $\|f(x^{k+1})\|_\infty$.

In fact, the Jacobian matrix need not be inversed: the new estimate x^{k+1} shall be the solution of the linear system

$$J_f(x^k) \cdot x^{k+1} = J_f(x^k) \cdot x^k - f(x^k)$$

that can be obtained through standard linear algebra algorithms:

- Direct methods like LU factorization
- Indirect methods (Gauss-Seidel, Successive Over Relaxation, BiConjugate Gradient, Generalized Minimal Residual...) that search iteratively the solution

The original SPICE simulator from Berkeley uses the Newton-Raphson algorithm, with several enhancements that were done either by Berkeley or by commercial software teams.

The One Step Relaxation algorithm

This algorithm was presented in the article [HSC85]. It replaces the global solving of a set of nonlinear equations by a Gauss-Seidel like iteration:

1. Start with an initial guess x^0
2. For each of the $i = 1, \cdots n$ equations, solve by the secant method the i^{th} equation:
$$f_i(x_1^{k+1}, \cdots, x_{i-1}^{k+1}, x_i^{k+1}, x_{i+1}^k, \cdots, x_n^k) = 0$$
with respect to the single unknown x_i^{k+1}.
3. Check for convergence on x^{k+1} estimate

Rem: the ELDO simulator from Mentor Graphics is based on this algorithm.

Convergence problems with stiff characteristics components

The exponential characteristic of the diode (or the quadratic response of a MOS transistor to V_{GS} when it goes from the weak inversion region to the strong inversion region) may cause convergence problems when a DC analysis tries to find an equilibrium point belonging to a region different from the initial guess, or when a transient analysis tries to compute the evolution of the device's current across two regions.

This will be illustrated in the case of the diode when the Newton-Raphson algorithm tries to find two successive polarization points of a circuit with a voltage source $E(t)$, a resistor R and a diode D (see Figure 2.3 for circuit's description and Figure 2.4 for algorithm).

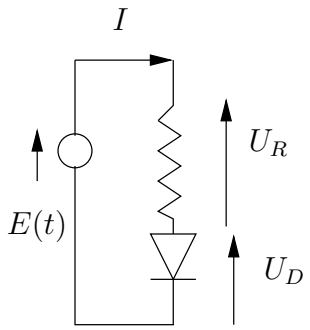


Figure 2.3: Polarization of a diode

The process for finding the new polarization point at time $t+h$ starts with as initial guess $U_D^0(t+h)$ the polarization point obtained for time t : $U_D(t)$. The first iterate $U_D^1(t+h)$ is given by the intersection between the tangent to the diode's characteristic and the source-resistor characteristic. Due to the stiffness of the diode's characteristic, this value $U_D^1(t+h)$ will result in a numerical overflow during the computation of the next iterate $U_D^2(t+h)$.

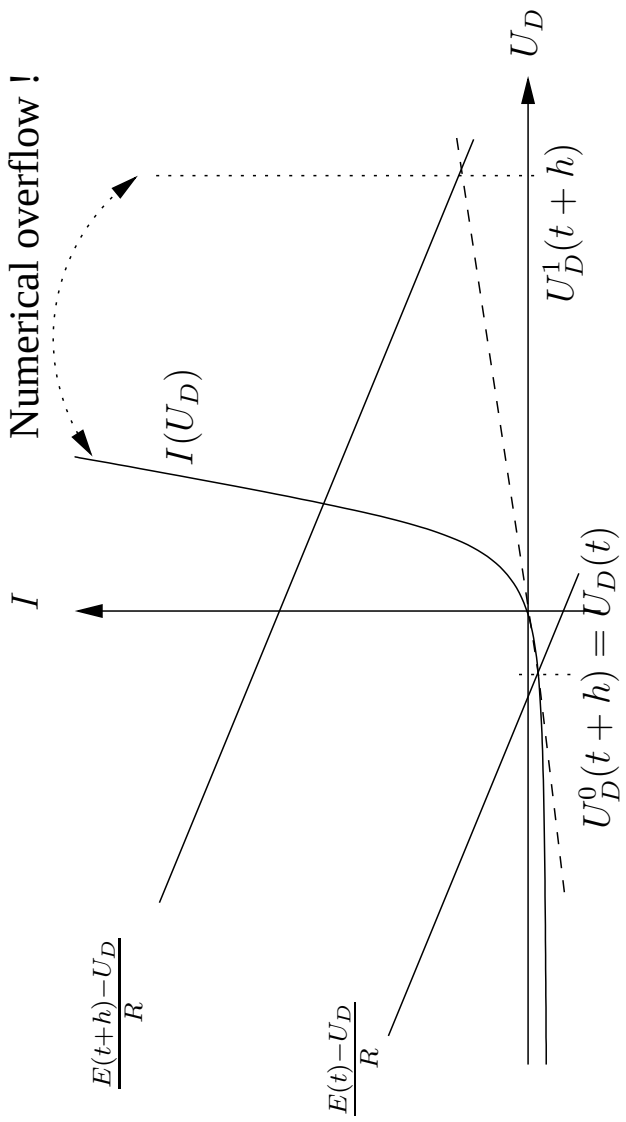


Figure 2.4: Newton-Raphson algorithm searching for a new polarization

Several solutions try to overcome these problems, yielding an increase of the number of iterations. Note that the secant method replacing Newton-Raphson algorithm is also prone to such drawback.

Remark 2 *The huge number of iterations required to compute the solution of a set of nonlinear equations is a key problem when one wants to simulate a circuit involving a large number of components with stiff characteristics for a large number of cycles. This is the case for instance in power electronics.*

2.3.2 Numerical integration of differential algebraic equations

The solution of ordinary differential equation $x' = f(x,t)$ over the time is obtained thanks to one of these standard integration methods, expressed for a time step h:

Implicit Euler : $x_{n+1} = x_n + h \cdot f(x_{n+1}, t_{n+1})$

Trapezoidal rule : $x_{n+1} = x_n + \frac{h}{2} \cdot (f(x_n, t_n) + f(x_{n+1}, t_{n+1}))$

2^{nd} **order backward differentiation formula :** $x_{n+1} = \frac{4}{3}x_n - \frac{1}{3}x_{n-1} + \frac{2h}{3} \cdot f(x_{n+1}, t_{n+1})$

all of them yielding a nonlinear equation with x_{n+1} as the unknown.

For a DAE system $f(x', x, t) = 0$, the same formulae may be applied to the equations where derivative terms appear, whereas the other equations without derivatives are straightly written at time t_{n+1}. For a complete study of DAE solvers and the associated notion of *index*, see [BCP95].

These methods were chosen for their good convergence/complexity tradeoff. The time step is usually automatically adjusted during the simulation in function of the solution's variation rate and of the difficulty to solve the nonlinear equation in x_{n+1}.

When some components of the circuit encounter a change in their region of operation (for instance, a blocked diode becoming passing), the time step must be reduced by large factors to enable the solving of the nonlinear implicit equations. This results in a considerable amount of CPU time spent.

Chapter 3

Recent approaches to the fast simulation of large circuits

As stated in the introduction, the standard SPICE simulators cannot achieve the simulation of circuits with more than hundreds of thousands of transistors. For the past decades, this was not an issue: large circuits are logic circuits, i.e an assembly of a large number of logic gates, each gate being itself an assembly of less than 100 transistors. Since the global behavior of a single gate could be modelled as an $OUT = f(IN)$ function with an associated delay and the interconnections behavior could also be modelled as a simple delay, thus designers had just to use SPICE to simulate each kind of logic gate in various conditions and extract the delay's parameters. The whole circuit could then be simulated with a logic simulator consisting basically in an event-driven algorithm. Of course, electrical parasitic phenomena could not be simulated but they used to be negligible. Sometimes, people had to simulate the interaction between pure analog parts of the circuit and pure logic ones: mixed simulators handle this task by running together a logic simulator and a time domain simulator with a coupling algorithm.

Today, people need to simulate those electrical parasitic phenomena linked to coupling between lines, propagation of waves along lines, variation of power levels both spatially and temporally. These phenomena may appear everywhere in a large circuit and the simulation task requires new tools.

Several software companies propose "fast SPICE" simulators that use some of the following tricks:

Mixing time-domain and event-driven simulations: people try to benefit from the intended behavior of logic gates as an $OUT = f(IN)$ function at various levels of modelling. The logic gates are not represented as black boxes like in a pure logic simulator, but the transistors netlist is analyzed to make a structure of dependencies appear and to order the evaluation of unknowns.

For instance, the `Nanosim` simulator from `Synopsys` (see [HZDS95]) or `Mach TA` from

`Mentor Graphics` use this approach.
Time-domain simulation can be used for improving the accuracy of small structures simulation and event-driven simulation is applied to simulate the relations between them. Somehow, it looks like the older approach but instead of doing once the time-domain simulation of logic gates and using thereafter the extracted delays, people do it in a dynamical way during a global simulation.

Mixing time-domain and frequency-domain simulations: the simulation of transistors and large RLC networks extracted from layout takes a long time with a standard SPICE kernel. The idea is then to mix a standard SPICE solver with a frequency-domain solver that is best suited to analyze large RLC networks response to high frequency signals.
For instance : `NSPICE` from `Apache Design Solutions`.

Benefitting from the hierarchy and the repetitive structures: the electronic circuits are designed as an assembly of blocks that should interfere only through their ports. Instead of flattening the whole circuit at the transistor level, it is preferable to keep track of this hierarchy during a simulation since it allows to solve large systems not as a whole but on a block basis. Moreover, some blocks may behave very closely since their internal structure is the same: some evaluation steps may be done just once. Some of these concepts are used when mixing time-domain and event-driven simulations (see above) but they may also be used in a more general way.
For instance: `Virtuoso Ultrasim` from `Cadence`.

Using simplified models of transistors: From a simple switch with a RC up to a piewise linear approximation of the characteristic, people tried to provide faster simulation of transistors by dealing with the complex formulae of classical SPICE models. Sometimes, the model is so simple that it becomes possible to perform an event-driven simulation of the circuit at the transistor level while piecewise linear models intend to avoid the solving of nonlinear equations. Many CAD vendors propose such simplified models.
For instance, `Nanosim` from `Synopsys` or `the SWIFT mode of Dolphin's SMASH`.
The transition between regions of the piecewise linear approximation is forced to be continuous by allowing only small increases of the variables. This results usually in small time steps when a change of segment occurs. This approach will be discussed in chapter 4 where a rigorous mathematical framework for piecewise linear modelling is presented.

The first three approaches suit well to circuits that can be split in different parts that will be simulated with one or more adapted algorithms, provided that their interactions will not be too complex to achieve the simulation of the whole circuit by merging all sub-results easily. When these interactions forbid to split the circuit into blocks and thus oblige to simulate the whole circuit with a single algorithm, only the last solution, i.e the simplification of the models, can provide significant savings in computation time.

The problem is then how to do it, by providing new models and algorithms that will ensure the best speed-accuracy trade-off. In the following chapter, the non-smooth approach to modelling and simulating systems is presented as a good candidate.

Chapter 4

The non-smooth approach to modelling and simulating electronic circuits in time-domain

4.1 The mathematical framework of the non-smooth approach

The non-smooth approach [1] is the application of a special field of mathematics that enables to represent relations between variables not as functions $y = f(x)$ but as complementarity conditions, for instance:

$$(x \geq 0) \text{ and } (y \geq 0) \text{ and } (x \cdot y = 0)$$

that is usually written this way:

$$0 \leq x \perp y \geq 0$$

This example is particularly interesting since it describes the ideal diode characteristic.

On Figure 4.1, the left-hand sketch displays the ideal diode characteristic and the right-hand sketch displays the usual exponential characteristic as stated by Shockley's law.

The possible values for $(i_D, -v_D)$ as depicted by this sketch is a complementarity condition:

$$0 \leq i_D \perp -v_D \geq 0$$

[1] For more information on this subject, one can refer to the site `http://siconos.inrialpes.fr/`

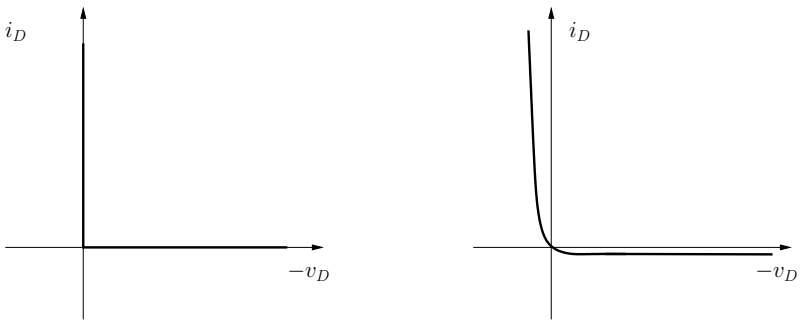


Figure 4.1: Non-smooth and smooth characteristics of a diode

When a linear relation is added between the complementary variables, one gets a linear complementarity problem (LCP) that is usually written as:

$$\begin{gathered} w = M \cdot z + q \\ 0 \leq w \perp z \geq 0 \\ \text{with } w, z, q \in \mathbb{R}^n \end{gathered}$$

where $z \geq 0$ means that $z_i \geq 0 \qquad \forall i \in \{1 \cdots n\}$

For instance, the circuit of Figure 2.3 may be written:

$$\begin{gathered} -v_D = Ri_D - E \\ 0 \leq i_D \perp -v_D \geq 0 \end{gathered}$$

Solving this mathematical problem seems at first glance obvious with a single diode but in a circuit containing thousands of diodes, the task might be more difficult: at first, one could try to solve the linear equation of the LCP assuming that the diode is either blocked ($i_D = 0$) or passing ($v_D = 0$). With n diodes in a circuit, the LCP is of size n and the number of tests is then 2^n. In fact, optimization theory has provided algorithms that use to solve the LCP much faster (see [CPS92]).

The LCP can also be applied to model more complex characteristics. For instance, any piecewise linear function can be modelled as a LCP (see [LVB98]). For instance, let's consider the function of a real variable x (Figure 4.2):

$$y = f(x) = \begin{cases} a_1 \cdot x + b & \text{if } x < 0 \\ a_2 \cdot x + b & \text{if } x \geq 0 \end{cases}$$

It can also be written as a LCP parameterized by x:

$$y = a_2 \cdot x + (a_2 - a_1) \cdot z + b \tag{4.1}$$

$$w = z + x \tag{4.2}$$

$$0 \leq w \perp z \geq 0 \tag{4.3}$$

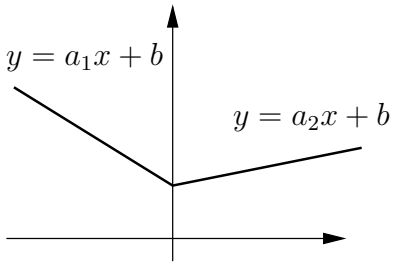


Figure 4.2: Piecewise linear function

For each x, the solution of the LCP (4.2) and (4.3) yields $z = -x$ if $x < 0$ and $z = 0$ if $x \geq 0$. The value of y can then be computed.

The advantage of the implicit form of a piecewise linear model appearing when it is written as a LCP is that it can be mixed with non functional relations like the ideal diode model, the global system being solved with LCP algorithms.

Up to that point, we have presented the LCP formulation as a tool to model and solve implicit relations between variables. When one wants to analyze the behavior of an electronic circuit, it is necessary to introduce dynamics in the descriptions, leading to consider non-smooth dynamical systems. The study of these systems started historically in the field of mechanics ([Mor66] and [Bro99]).

4.2 Simulation results and comparisons: power electronics

4.2.1 The example of the RLCD circuit of Figure 2.2 as a non-smooth dynamical system

We will see now how to model the RLCD circuit of Figure 2.2 as a non-smooth dynamical system and how it can be simulated thanks to an adequate time-integration method and a LCP solver.

We first rewrite the Kirchhoff laws:

$$\begin{aligned} v_L &= v_C \\ v_R + v_D &= v_C \\ i_C + i_L + i_R &= 0 \\ i_R &= i_D \end{aligned}$$

while the branch constitutive equations for linear devices are:

$$\begin{aligned} i_C &= Cv'_C \\ v_L &= Li'_L \\ v_R &= Ri_R \end{aligned}$$

and last the "branch constitutive equation" of the ideal diode that is no more an equation but instead a complementarity condition:

$$0 \leq i_D \perp -v_D \geq 0$$

After rearranging the previous equations, we obtain:

$$\begin{pmatrix} v_L' \\ i_L' \end{pmatrix} = \begin{pmatrix} 0 & \frac{-1}{C} \\ \frac{1}{L} & 0 \end{pmatrix} \cdot \begin{pmatrix} v_L \\ i_L \end{pmatrix} + \begin{pmatrix} \frac{-1}{C} \\ 0 \end{pmatrix} \cdot i_D$$

We introduce a state variable x and one of the complementary variables λ:

$$x = \begin{pmatrix} v_L \\ i_L \end{pmatrix}$$

and

$$\lambda = i_D$$

The initial condition of the system is given by:

- The initial value of the inductor voltage $v_L = x_1^0$
- The initial value of the inductor current $i_L = x_2^0$

Rearranging further the initial set of equations yields:

$$-v_D = \begin{pmatrix} -1 & 0 \end{pmatrix} \cdot \begin{pmatrix} v_L \\ i_L \end{pmatrix} + Ri_D$$

as a linear relation between the state variable x and the complementary variables λ and y with $y = -v_D$.

The complementarity condition resulting from the ideal diode characteristic is written :

$$0 \leq i_D \perp -v_D \geq 0$$

With the general notation x, λ, y the system is written:

$$x' = A \cdot x + B \cdot \lambda \tag{4.4}$$

$$y = C \cdot x + D \cdot \lambda \tag{4.5}$$

$$0 \leq y \perp \lambda \geq 0 \tag{4.6}$$

with A, B, C, D matrices constant over time.

The theory of non-smooth dynamical systems provides integration techniques that have been implemented in the SICONOS software to obtain the results of Figure 4.3 which shows also a comparison with the results of a SPICE simulator. The diode used in SPICE simulation had a threshold of around 0.21 V, this threshold was also simulated with SICONOS thanks to a slight modification of previous equations and variables. *The SICONOS software is a toolbox that is currently under development through a European project headed by INRIA and dedicated to the modelling, simulation and control of nonsmooth dynamical systems (Web page* ***http://siconos.inrialpes.fr/****).*

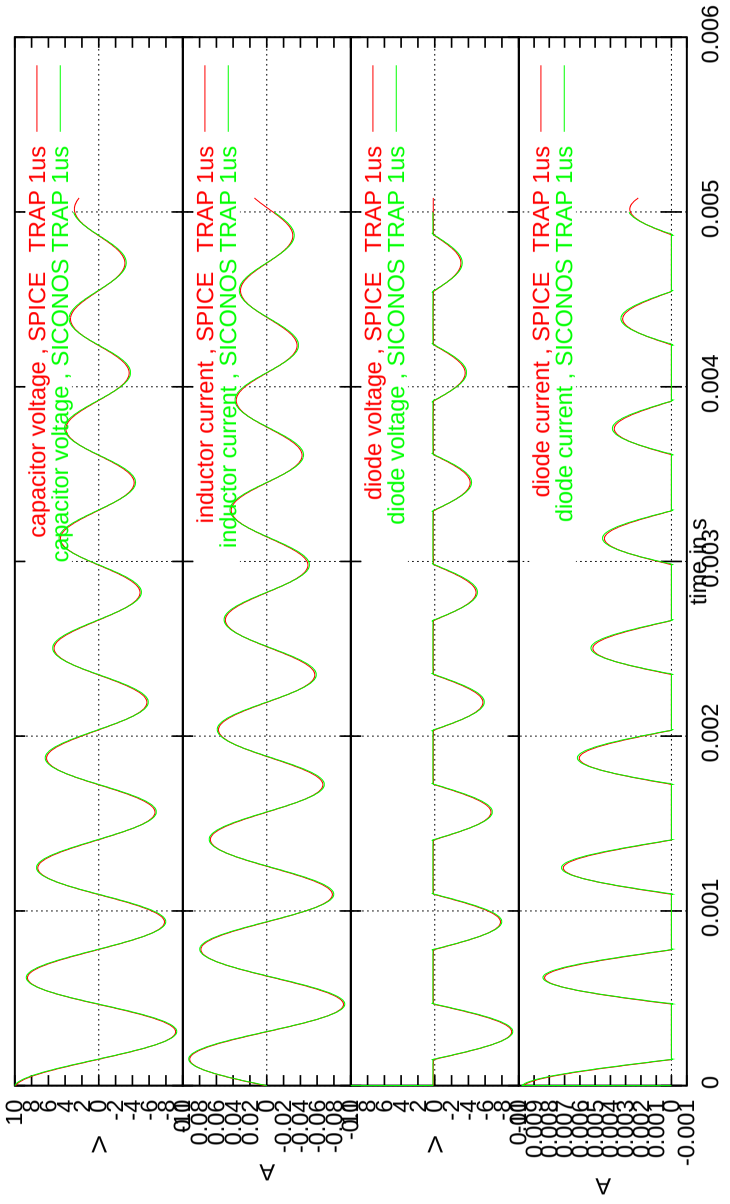


Figure 4.3: SPICE and SICONOS simulation results of RLCD circuit, 1 μs time step

4.2.2 Diodes bridge circuit simulation

A little bit more complex example was simulated: a sinusoidal voltage supply providing energy to a resistor through a 4 diodes bridge full-wave rectifier filtered with a capacitor (see Figure 4.4).

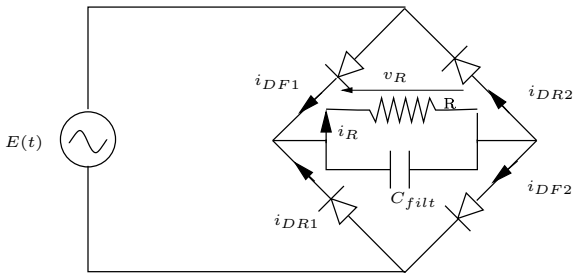


Figure 4.4: Filtered full-wave rectifier

The figures 4.5 , 4.6 and 4.7 show what happens with the SPICE algorithms when the time step is forced to a "high value" (here 10μs): the SPICE simulator seems to converge but the results are erroneous while the non-smooth approach provides accurate results.

The figures 4.8 and 4.9 show a comparison between SPICE results with a time step of 0.1μs and SICONOS results with respectively time steps of 2μs and 1μs. The 2μs results are already very close to SPICE ones, whereas at 1μs the differences are almost unnoticeable, whereas a factor of 10 is gained on the time step.

These results suggest that with a small number of stiff components in a circuit, the convergence of the Newton-Raphson algorithm is already impaired, even if several tricks were added in the SPICE software to help it. When the integration time period becomes too large, some diodes may be completely blocked at a time step and completely passing at the next time step. The SPICE algorithms are not designed to handle such a case: they need to step a sufficient number of times to cover properly all the switching period which is very short here.

On the contrary, the non-smooth approach is able to compute a consistent solution with relatively far time steps, assuming that it exists and it is unique, which is true here.

4.2.3 Power converters

The functioning of switch mode power supplies is based on flyback diodes and switched transistors with a regulation on output current or voltage. The article [BFMM05] presents simulation results of a Cuk converter [2].

[2]This work was supported by the European project SICONOS IST-2001-37172.

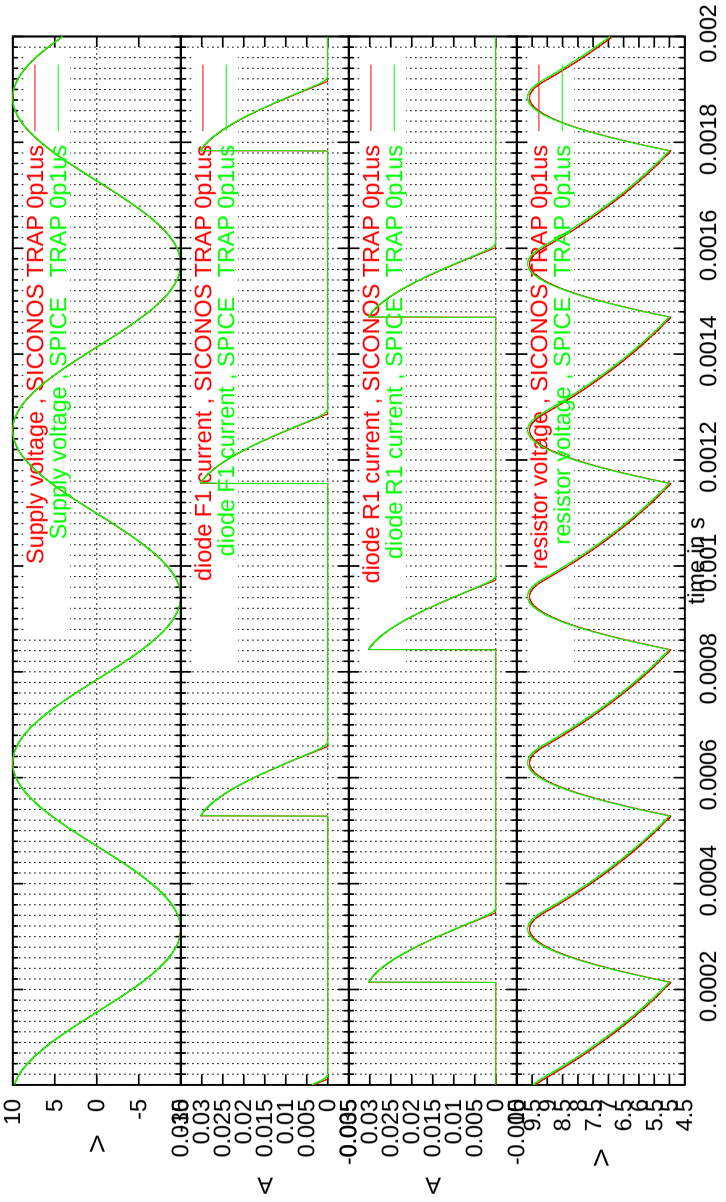


Figure 4.5: SPICE and SICONOS simulations of the diode bridge circuit, 0.1μs time step

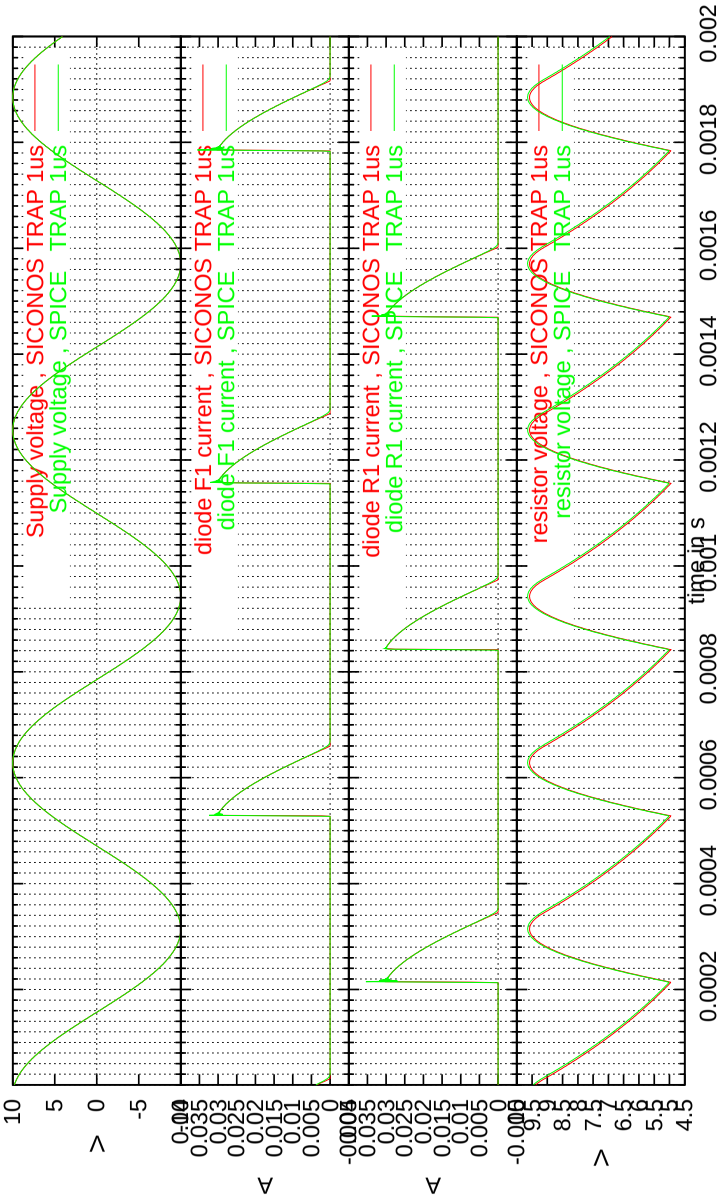


Figure 4.6: SPICE and SICONOS simulations of the diode bridge circuit, 1 μs time step

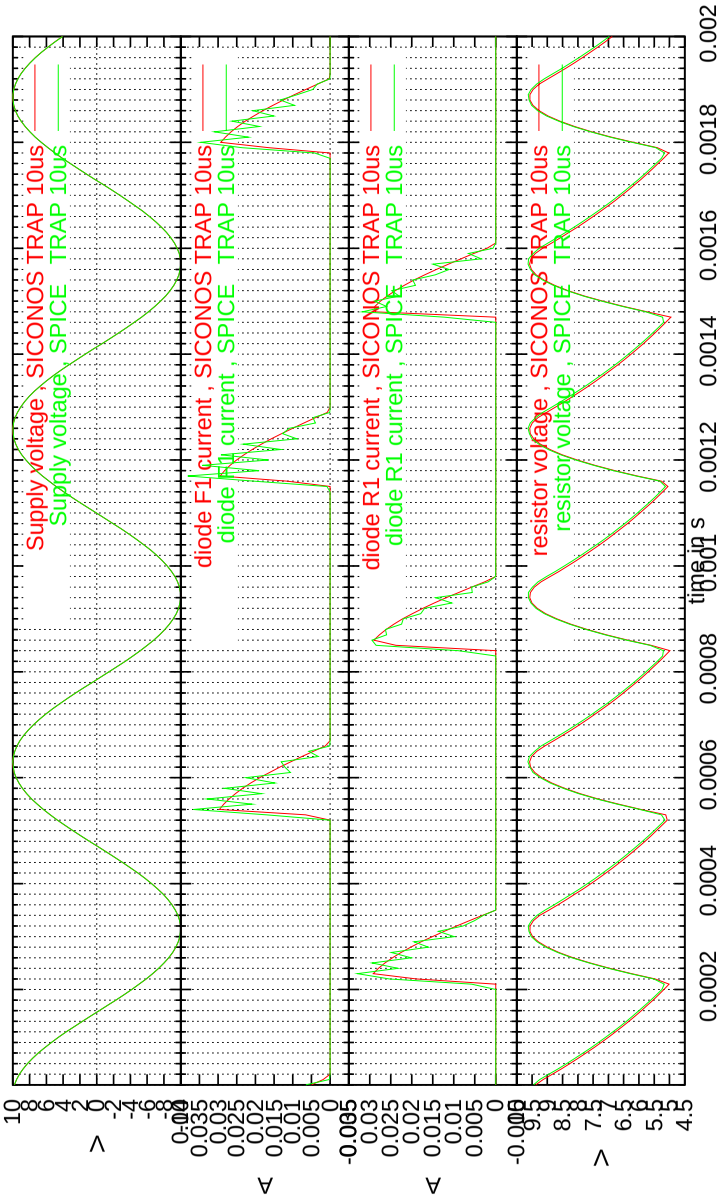


Figure 4.7: SPICE and SICONOS simulations of the diode bridge circuit, 10 μs time step

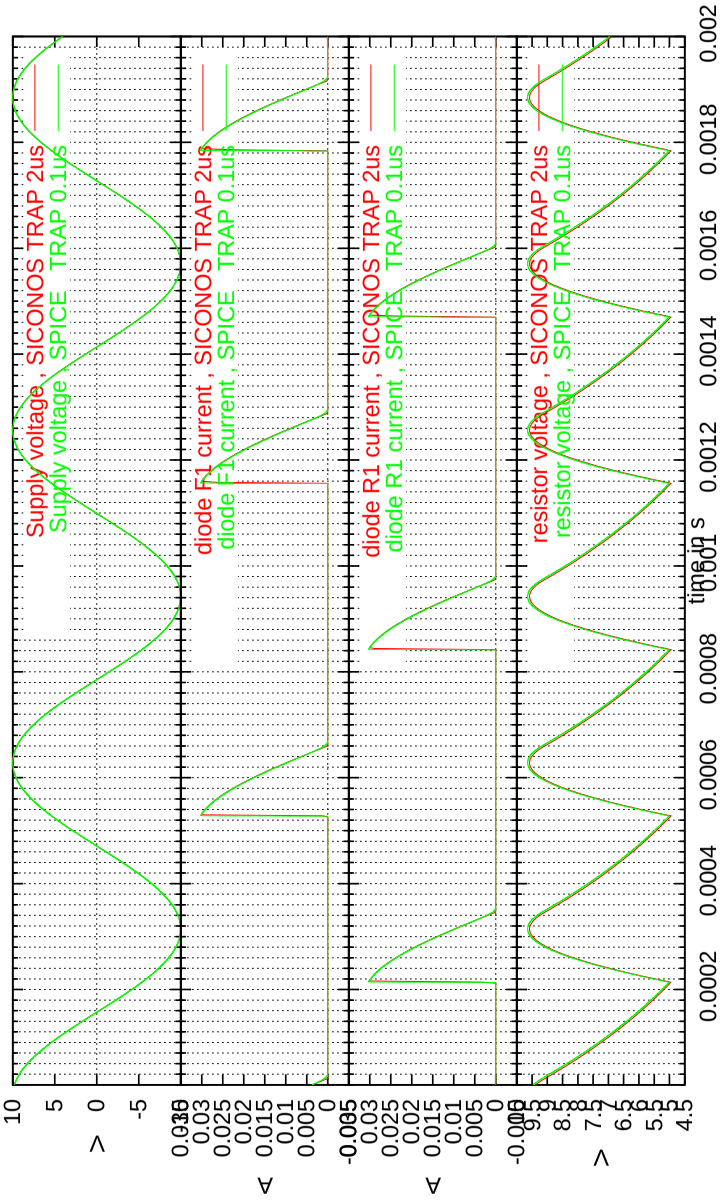


Figure 4.8: SPICE 0.1μs and SICONOS 2μs simulation results of the diode bridge circuit

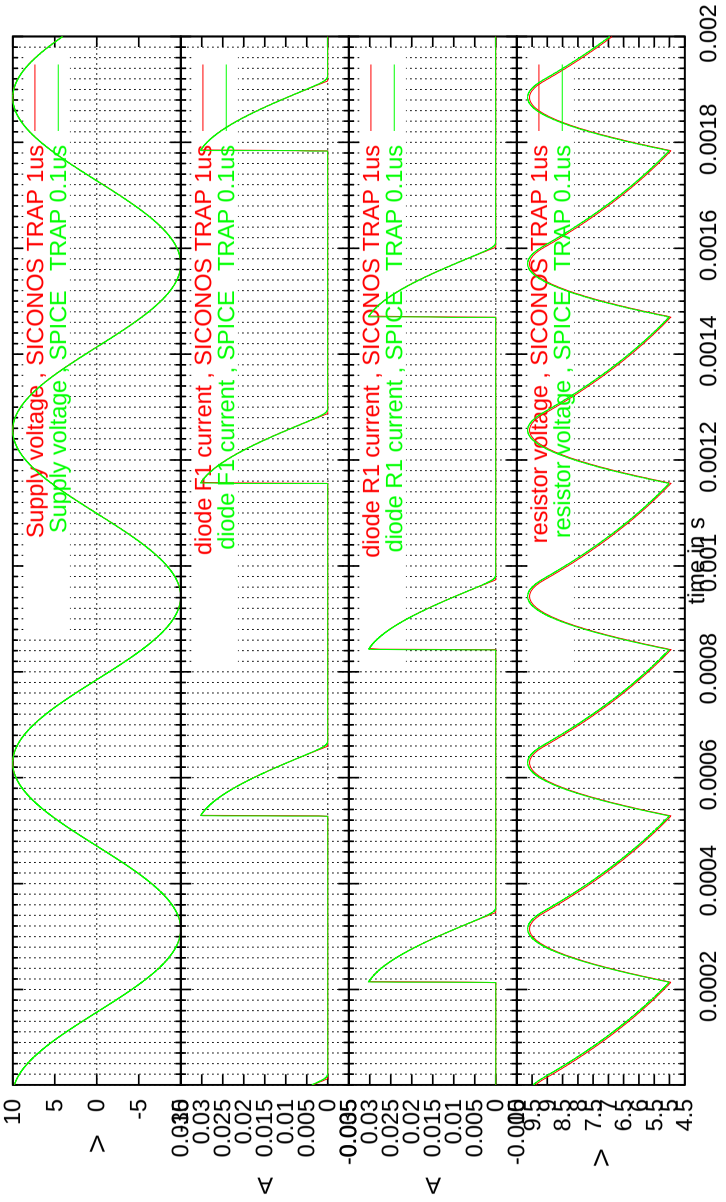


Figure 4.9: SPICE 0.1μs and SICONOS 1μs simulation results of the diode bridge circuit

4.3 Simulation results and comparisons: MOS transistors and inverters

Electronic circuits made of millions of MOS transistors are common today. As explained in the introduction part, the design of these circuits has long relied on a hierarchy of models and simulations:

- small subsets of tens of transistors implementing a given function - named logic gates - were simulated in given conditions in time domain with SPICE
- some useful parameters like delays were extracted from these simulations to fill a coarse model of the logic gate like a logic relation $OUT = f(IN1, IN2, \ldots)$ after delay T
- assemblies of a large number of logic gates could be simulated in various conditions with a fast event driven simulator, the results being accurate enough to predict the behavior of the circuit.

The evolution of semiconductor technologies toward smaller transistor size and faster operation requires to simulate parasitic effects that used to be negligible before. Unfortunately, some of these effects like crosstalk between lines cannot be handled at the logic gate level but require to simulate in time domain the full circuit. Doing it with SPICE would require months to reach a single result, with a very high but maybe unnecessary precision.

4.3.1 Piecewise linear model of a MOS transistor

People could benefit from a simplification of devices models (e.g MOS models) in the form of a piecewise linear representation instead of the complicated formula implemented in SPICE simulators. For instance, in [LVB98], the authors considered the Sah model of the NMOS static characteristic:

$$I_{DS} = \frac{K}{2} \cdot (f(V_G - V_S - V_T) - f(V_G - V_D - V_T))$$

with:

$K = \frac{\mu C_{OX} W}{L}$

μ mobility of majority carriers

(sample values of 750 $cm^2.V^{-1}.s^{-1}$ for a NMOS, 250 $cm^2.V^{-1}.s^{-1}$ for a PMOS)

$C_{OX} = \frac{\epsilon_{SiO_2}}{t_{OX}}$

$\epsilon_{SiO_2} = \epsilon_{r\ SiO_2} \cdot \epsilon_0$ ($\epsilon_{r\ SiO_2} \approx 3.9$)

t_{OX} oxide thickness $\approx 4nm$ in a recent $180nm$ technology

W channel width

L channel length $\approx 130nm$ in a recent $180nm$ technology

V_T threshold voltage depending on technology, V_{BS} , temperature ≈ 0.25 to 1 V

The function $f : \mathbb{R} \longrightarrow \mathbb{R}$ is defined as:

$$f(x) = \begin{cases} 0 & \text{if } x < 0 \\ x^2 & \text{if } x \geq 0 \end{cases}$$

The piecewise and quadratic nature of this function was approximated by the following 6 segments piecewise linear function by the authors of [LVB98] (see Figure 4.10):

$$f_{PWL}(x) = \begin{cases} 0 & \text{if } x < 0 \\ 0.09 \cdot x & \text{if } 0 \leq x < 0.1 \\ 0.314055 \cdot x - 0.0224055 & \text{if } 0.1 \leq x < 0.2487 \\ 0.780422 \cdot x - 0.138391 & \text{if } 0.2487 \leq x < 0.6185 \\ 1.94107 \cdot x - 0.856254 & \text{if } 0.6185 \leq x < 1.5383 \\ 4.82766 \cdot x - 5.29668 & \text{if } 1.5383 \leq x \end{cases}$$

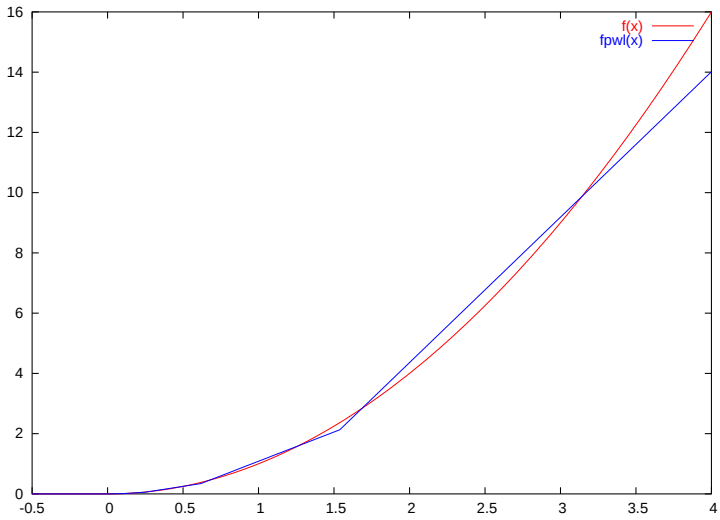


Figure 4.10: Piecewise linear approximation of f

The relative error between f and f_{PWL} is kept below 0.1 for $0.1 \leq x < 3.82$. The absolute error is less than $2 \cdot 10^{-3}$ for $0 \leq x < 0.1$ and 0 for negative x. In practice, the values of V_G, V_S, V_D, V_T in logic integrated circuits allow a good approximation of f by f_{PWL}.

The figure 4.11 displays the static characteristic $I_{DS}(V_{GS}, V_{DS})$ of an NMOS obtained with the SPICE level 1 model and the piecewise linear approximation of the Sah model. The following parameter values were used:

$$\epsilon_{r\ SiO_2} = 3.9$$
$$t_{OX} = 20\ nm$$
$$\mu = 750\ cm^2.V^{-1}.s^{-1}$$
$$W = 1\ \mu m$$
$$L = 1\ \mu m$$
$$V_T = 1\ V$$

Bottom figures include both models results with two different viewpoints to display the regions where differences appear.

The largest differences occur for large V_{DS} and either a large positive V_{GS} or a large positive V_{GD}. Indeed this yields a high value of x in one of the $f(x)$ in $f(V_{GS} - V_T) - f(V_{GD} - V_T)$ and the linear approximation f_{PWL} differs from f. For small values of V_{DS}, errors compensate due to the difference $f(V_{GS} - V_T) - f(V_{GD} - V_T)$.

For simulating CMOS logic circuits, the useful operating region is the square $(V_{GS}, V_{DS}) \in [0, 5]^2$ and the error is moderate.

The piecewise linear model results on Figure 4.11 were reached by a LCP algorithm. It means that the definition of f_{PWL} is turned into an LCP formulation as explained in 4.1. For a given value of (V_D, V_G, V_S), the λ values corresponding to the intervals in which $V_{GS} - V_T$ and $V_{GD} - V_T$ fall are computed, allowing then to compute I_{DS}.

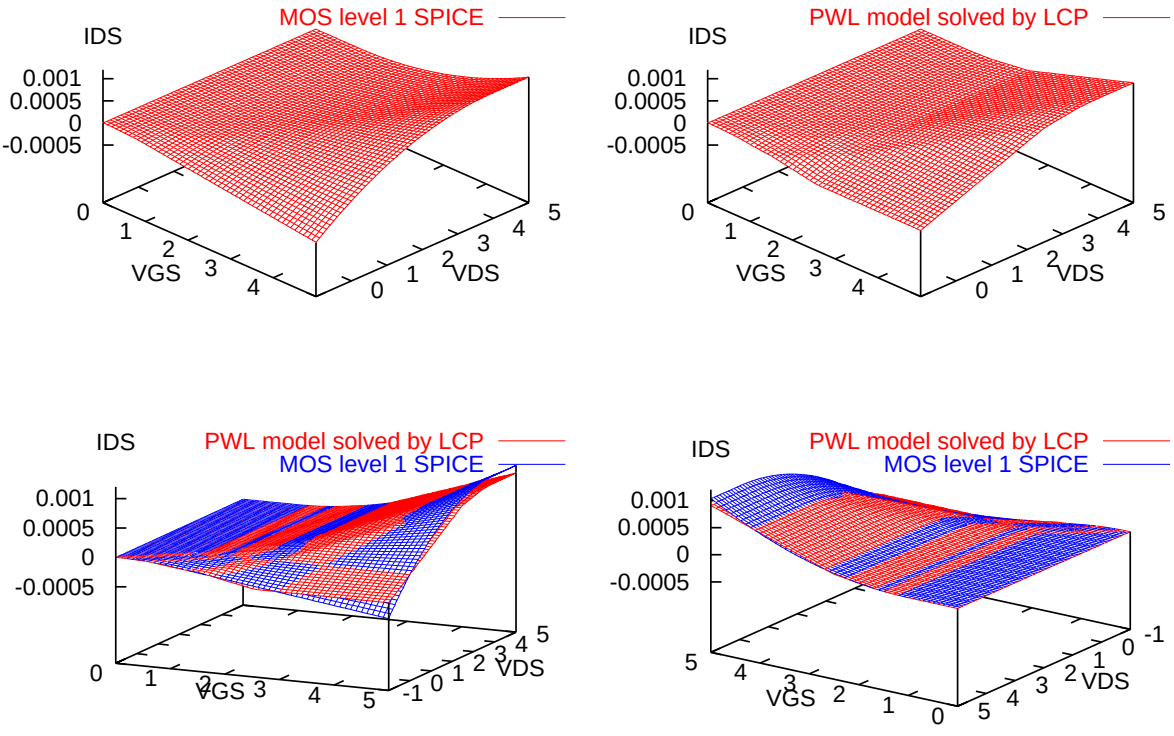


Figure 4.11: Static characteristic of an NMOS transistor with a simple PWL model and SPICE level 1 model

4.3.2 Inverter chain

This simple model of a NMOS transistor was adapted to the PMOS transistor and both models were used to simulate an inverter chain (see Figure 4.12). The output of each inverter is loaded by the intrinsic capacitances of transistors (with values of a few fF) and a load capacitor of 50 fF representing the wiring between successive inverters.

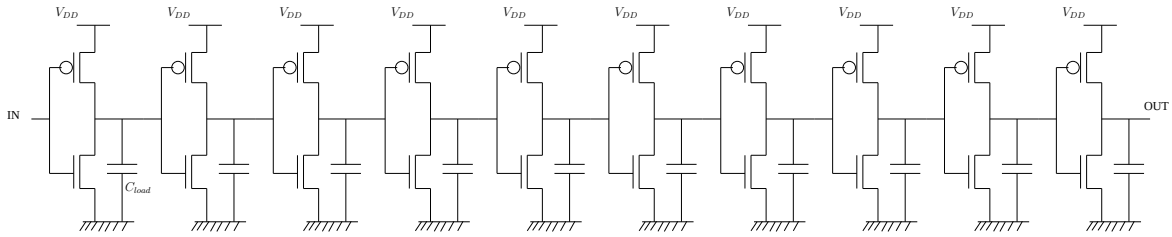


Figure 4.12: Inverter chain in CMOS

In these early simulations, the dynamical behavior of the MOS transistor was simplified by keeping the intrinsic capacitances C_{GS} and C_{GD} independent from voltages. Of course, this differs from the Meyer nonlinear capacitances implemented in the SPICE level 1 model. Figure 4.13 shows the comparison between simulation results with SPICE (dotted lines) and SICONOS for a selection of inverters output voltage and MOS currents. Figures 4.14 and 4.15 display the (V_{GS}, V_{DS}, I_{DS}) values for inverters 1 and 9 computed during the transient simulation superimposed on the NMOS static characteristics $I_{DS}(V_{GS}, V_{DS})$ of SPICE and SICONOS. We can notice that the switching of these inverters are located mainly in a region where the I_{DS} current given by the PWL model exceeds the one given by SPICE, partly explaining why the inverter delays are smaller with SICONOS.

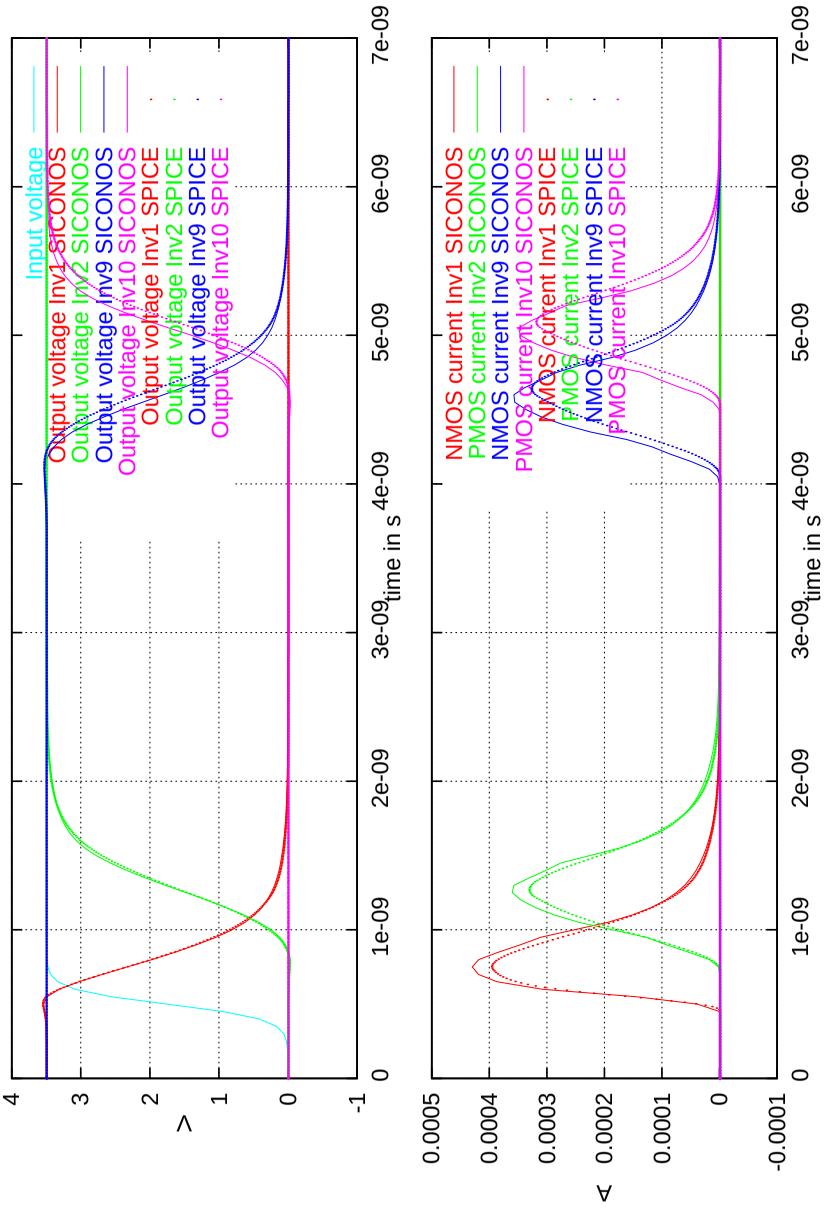


Figure 4.13: Simulation of a 10 inverters chain with SICONOS and SPICE level 1 model

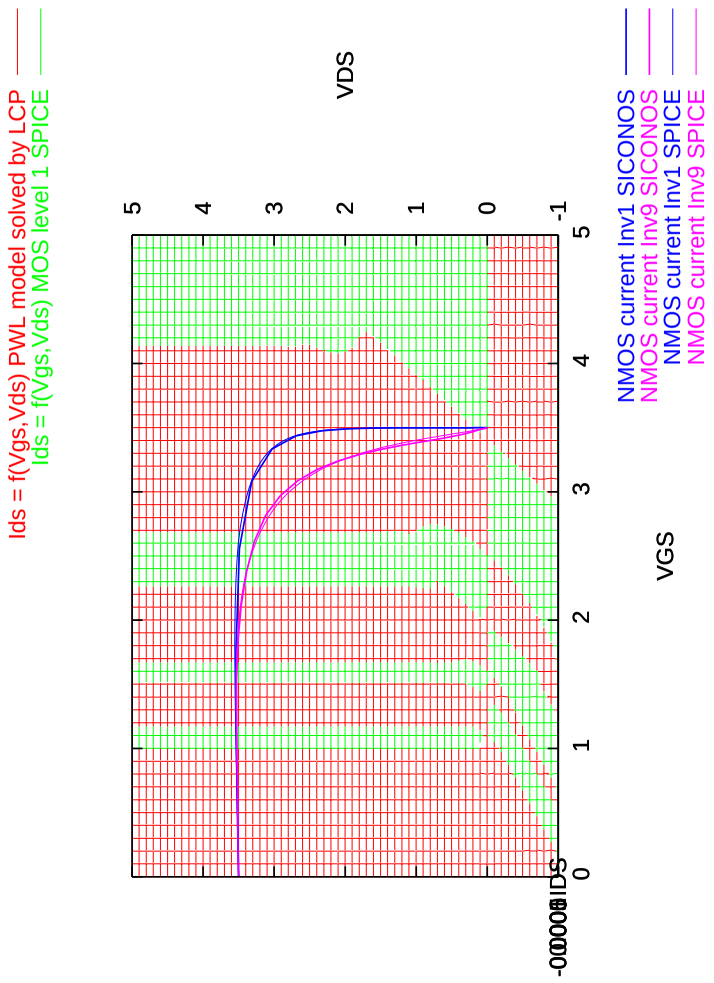


Figure 4.14: Plot of (V_{GS}, V_{DS}, I_{DS}) values for inverters 1 and 9 and NMOS characteristics (top view)

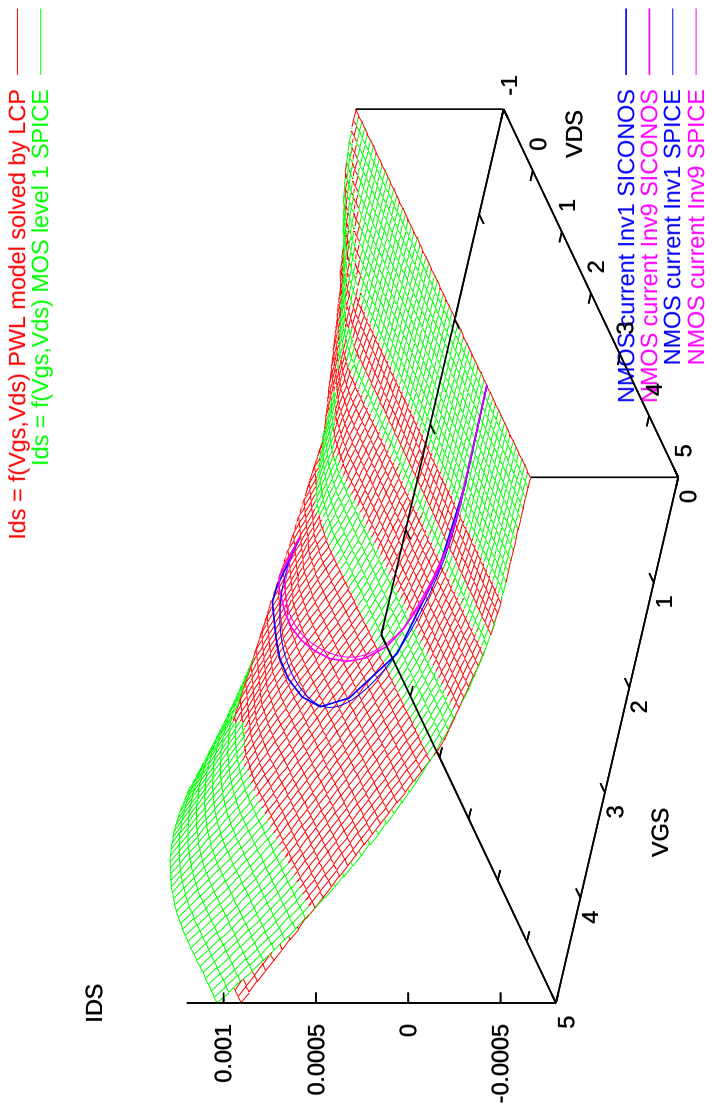


Figure 4.15: Plot of (V_{GS}, V_{DS}, I_{DS}) values for inverters 1 and 9 and NMOS characteristics (perspective view)

Chapter 5

Conclusion

The design of integrated circuits containing millions of transistors and affected by analog effects requires a new generation of time-domain simulators. Some products already exist but they are based on a mixture of classical solving algorithms applied to approximate device models.

The non-smooth approach based on a radically different mathematical framework has been tried to solve simple electrical circuits exhibiting fast transitions. It was shown that when the time step is forced to be large, the SPICE algorithms may converge to erroneous solutions, whereas the non-smooth approach still provides acceptable results.

The non-smooth approach is being developed at INRIA through both theoretical studies on algorithms and implementation of a general software toolbox (SICONOS). After first successful experiments carried on simple electronic circuits, a complete simulator will be developed. The main issues to be solved are:

- an automated equation formulation turning a netlist into a non-smooth complementarity system. The careful choice of state and complementary variables shall allow to solve the complementarity problem at each time step.
- the derivation of non-smooth or piecewise linear models of electronic devices from their precise characteristic with a good accuracy/compaction trade-off.

Bibliography

[BCP95] K. E. Brenan, S. L. Campbell, and L. R. Petzold. *Numerical Solution of Initial-Value Problems in Differential-Algebraic Equations.* SIAM, 1995.

[BFMM05] C. Batlle, E. Fossas, I. Merillas, and A. Miralles. Generalized discontinuous conduction modes in the complementarity formalism. *Circuits and Systems II: Express Briefs, IEEE Transactions on*, 52, no.8:447–451, Aug. 2005.

[Bro99] Bernard Brogliato. *Nonsmooth Mechanics : Models, Dynamics and Control.* Communications and Control Engineering. Springer-Verlag, second edition, 1999.

[CPS92] R.W. Cottle, J.-S. Pang, and R.E. Stone. *The Linear Complementarity Problem.* Academic Press, New York, 1992.

[HBG71] G. Hachtel, R. Brayton, and F. Gustavson. The sparse tableau approach to network analysis and design. *IEEE Transactions on Circuits and Systems*, 18:101–113, 1971.

[HRB75] C.-W. Ho, A. Ruehli, and P. Brennan. The modified nodal approach to network analysis. *IEEE Transactions on Circuits and Systems*, 22:504–509, 1975.

[HSC85] B. Hennion, P. Senn, and D. Coquelle. A new algorithm for third generation circuit simulators: the one-step relaxation method. In *DAC '85: Proceedings of the 22nd ACM/IEEE conference on Design automation*, pages 137–143, New York, NY, USA, 1985. ACM Press.

[HZDS95] Charlie X. Huang, Bill Zhang, An-Chang Deng, and Burkhard Swirski. The design and implementation of `PowerMill`. In *ISLPED '95: Proceedings of the 1995 international symposium on Low power design*, pages 105–110, New York, NY, USA, 1995. ACM Press.

[LVB98] Domine M. W. Leenaerts and Wim M. Van Bokhoven. *Piecewise Linear Modeling and Analysis.* Kluwer Academic Publishers, Norwell, MA, USA, 1998.

[Mor66] J.-J. Moreau. Quadratic programming in mechanics: Dynamics of one-sided constraints. *SIAM J. Control*, 4:153–158, 1966.

[Nag75] L.W. Nagel. Spice2: A computer program to simulate semiconductor circuits. Technical Report ERL Memo No. ERL-M520, Electronics Research Laboratory, University of California, Berkeley, May 1975.

List of Figures

2.1 Electrical model of a diode 8
2.2 Electrical oscillator with half-wave rectifier 9
2.3 Polarization of a diode 14
2.4 Newton-Raphson algorithm searching for a new polarization 15

4.1 Non-smooth and smooth characteristics of a diode 22
4.2 Piecewise linear function 23
4.3 SPICE and SICONOS simulation results of RLCD circuit, 1 μs time step . . 25
4.4 Filtered full-wave rectifier 26
4.5 SPICE and SICONOS simulations of the diode bridge circuit, 0.1μs time step 27
4.6 SPICE and SICONOS simulations of the diode bridge circuit, 1 μs time step 28
4.7 SPICE and SICONOS simulations of the diode bridge circuit, 10 μs time step 29
4.8 SPICE 0.1μs and SICONOS 2μs simulation results of the diode bridge circuit 30
4.9 SPICE 0.1μs and SICONOS 1μs simulation results of the diode bridge circuit 31
4.10 Piecewise linear approximation of f 33
4.11 Static characteristic of an NMOS transistor 35
4.12 Inverter chain in CMOS 36
4.13 Simulation of a 10 inverters chain with SICONOS and SPICE level 1 model . 37
4.14 Inverters chain simulations and NMOS characteristics (top view) 38
4.15 Inverters chain simulations and NMOS characteristics (perspective view) . . . 39



Unité de recherche INRIA Rhône-Alpes
655, avenue de l'Europe - 38334 Montbonnot Saint-Ismier (France)

Unité de recherche INRIA Futurs : Parc Club Orsay Université - ZAC des Vignes
4, rue Jacques Monod - 91893 ORSAY Cedex (France)
Unité de recherche INRIA Lorraine : LORIA, Technopôle de Nancy-Brabois - Campus scientifique
615, rue du Jardin Botanique - BP 101 - 54602 Villers-lès-Nancy Cedex (France)
Unité de recherche INRIA Rennes : IRISA, Campus universitaire de Beaulieu - 35042 Rennes Cedex (France)
Unité de recherche INRIA Rocquencourt : Domaine de Voluceau - Rocquencourt - BP 105 - 78153 Le Chesnay Cedex (France)
Unité de recherche INRIA Sophia Antipolis : 2004, route des Lucioles - BP 93 - 06902 Sophia Antipolis Cedex (France)

Éditeur
INRIA - Domaine de Voluceau - Rocquencourt, BP 105 - 78153 Le Chesnay Cedex (France)
http://www.inria.fr
ISSN 0249-0803