New FPGA image-oriented acquisition and real-time processing applied to plasma facing component thermal monitoring

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New FPGA-based image-oriented acquisition and real-time processing applied to plasma facing component thermal monitoring[a)]

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During operation of present fusion devices, the Plasma Facing Components (PFCs) are exposed to high heat fluxes. Understanding and preventing overheating of these components during long pulse discharges is a crucial safety issue for future devices like ITER. Infrared digital cameras interfaced with complex optical systems have become a routine diagnostic to measure surface temperatures in many magnetic fusion devices. Due to the complexity of the observed scenes and the large amount of data produced, the use of high computational performance hardware for real-time image processing is then mandatory to avoid PFC damages. At Tore Supra, we have recently made a major upgrade of our real-time infrared image acquisition and processing board by the use of a new Field Programmable Gate Array (FPGA) optimized for image processing. This paper describes the new possibilities offered by this board in terms of image calibration and image interpretation (abnormal thermal events detection) compared to the previous system.

I. INTRODUCTION

One aspect of the tokamak protection function is to avoid irreversible plasma facing components (PFCs) degradation during long pulses to obtain high performance plasmas in the safest mode. In this context, infrared thermography is becoming a routine diagnostic in many magnetic fusion devices to monitor the heat loads on the PFCs as heating antennas or divertor. The good results of the developed systems obtained so far[1] motivate the intensive use of imaging diagnostics for real-time plasma control. As described in Travere et al.[2], a step towards automatic video understanding applied to qualitative plasma imaging analysis is now necessary to achieve safety tasks in future devices like ITER. Indeed, the camera network (36 infrared and visible views) planned for ITER will deliver data at a rate of about 10 Gb/s thus requiring development of high computational performance hardware for real-time integrated data analysis such as image calibration and interpretation. In this paper, we describe our new FPGA-based (Field Programmable Gate Array) image-oriented acquisition and real-time processing system applied to PFCs monitoring on the Tore Supra tokamak.

II. PFC REAL-TIME MONITORING SYSTEM ON TORE SUPRA

The infrared imaging system for PFC monitoring of Tore Supra is routinely used as input of a Plasma Control System (PCS) based on the early detection of local overheating areas to control in real time the heating power sources[1]. This unique PCS, made of seven endoscopes bodies equipped so far with eight infrared cameras, monitors the five heating antennas as well as two 30° sectors of the toroidal bottom limiter. The image analysis part of the PCS consists in detecting high increase of the infrared (IR) luminance signal beyond fixed qualitative levels for a set of predefined Region of Interest (ROIs) (see figure 1 left). The ROIs are defined according to the geometry of monitored components where characteristic thermal events (TEs) are observed as electrical arcing in front of LHCD (Low Hybrid Current Drive) copper mouth or impacts of accelerated electrons on the ICRH (Ion Cyclotron Resonance Heating) side protections. The thresholds associated to each ROI are set to maintain the surface temperature of the components within their technological limits. The raw data (320×242 12-bit pixels, 50Hz) of each IR camera sent via optic fibers to the electronic conditioning system are processed with a specific electronic board (Altera Acex LUMV). This board supplies in real-time the maximum value of luminance temperature in up to 16 predefined ROIs. The global transmission of the optical system (endoscope and sapphire window) is estimated in laboratory. The calibration procedure consists in subtracting the image of a black body acquired through the complete optical system from the image of the black body black acquired by direct camera sighting.

III. CURRENT ISSUES

Three major issues can be drawn from this first experience. First, the different material emissivities of the observed components - from 0.4 for copper and stainless steel to ~ 1 for carbon fiber composite - must be taken into account for the pixel-wise temperature estimation.

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Currently, the whole IR scene is assimilated to a black body (i.e. with $\epsilon = 1$) thus leading to an underestimation of surface temperature for some components (e.g. copper mouth of LHCD).

Second, the transfer function of the optical system (window transmission and optical assembly transmission factors) is not uniform in space and constant in time. For instance, the front-end sapphire window transmission function is continuously degraded by particle deposit during plasma discharges and a factor two has even been observed between the top ($\tau = 0.70$) and the bottom ($\tau = 0.35$) of one of them after six months of plasma operation. Once again, a 2D transmission matrix must be used in the transfer function instead of a simple scalar for a better temperature calibration of the observed scene against local transmission defects.

Third, the current ROI-based local overheating detection system described in section II is not able to deliver precise spatial location of detected overheating objects since the system does not return the location of the maximum temperature in the ROI. The second drawback is that several (different types of) TEs may occur in the same ROI (e.g. impact of fast particles and electrical arcing on the LHCD copper mouth) while only one TE can be detected using temperature thresholding.

IV. NEW IMAGE-ORIENTED ARCHITECTURE

A new intelligent computer vision-based system has been recently developed at Tore Supra for the automatic detection and identification of thermal events in IR videos. We refer the reader to Martin et al.[3] for details on system architecture and performance compared to the current ROI-based system. Until now, this system has been validated through a pure software implementation performing at 25 frames per second. Our aim is to transfer parts of the developed software onto dedicated accelerated hardware to reach real-time constraints imposed by the acquisition system (e.g. one frame processed in less than 20 ms).

The main idea is to clearly separate the knowledge of the TEs (e.g. geometrical description, temporal behaviour, etc.) from the image data. Such problem formalization leads to separate the processing tasks into two categories: the former concerns costly algorithms as image segmentation (i.e. to categorize pixels into foreground and background classes) representing 80% of the total processing time of each image on a general CPU. Since pixel-wise processing can be massively parallelized, the use of Field Programmable Gate Array (FPGA) is then clearly motivated to accelerate such tasks. The later deals with image interpretation (e.g. pattern recognition) from image segmentation results (e.g. a binary image of detected hot spots). These algorithms are currently coded in C++ language which provides a high degree of flexibility and control of the interpretation process.

The new image-based system is then composed of two interconnected layers sketched in figure 2:

- The hardware layer, based on a Xilinx Virtex-5 FPGA is dedicated to parallel processing of costly calculations as matrix computation (e.g. image calibration and temperature estimation) and image segmentation algorithms. On board RAM memory allows the storage of large amount of data (calibration matrices, image buffering, etc.). The FPGA also embeds a camera error handling module to handle potential data acquisition errors (e.g. bad frame transmission). The goal is to prevent incoherent results during the overheating detection step by skipping the frame.
- The software layer is dedicated to overheating identification. The goal is to recognize TEs by means of spatiotemporal pattern reconstruction and classification (see details in Martin et al.[3]).

A particular feature of the system is to embed a real-time feedback control of the hardware layer by the software layer. Depending on TE identification results, the segmentation algorithm parameters stored in the FPGA are then dynamically updated.

The two layers are interfaced through a Direct Memory Access (DMA) to minimize the data transfer time. The proposed architecture manages all these massive data parallelism in such a way that is seamless to any of the processing blocks.

V. PERFORMANCE ASSESSMENT

The previous system was mainly limited by its lake of embedded memory making impossible matrix computations as seen in Table I.

FPGA board	Altera Acex LUMV (2000) ×2	1 Xilinx Virtex-5 SMT351T (2009)
Internal RAM	100 Kb	10 Mb
Clock Speed (MHz)	Up to 200	Up to 550 (with embedded PLL)
On board Memory	1 x 1 MB SRAM	2 x 1 GB DDR2 SDRAM
DSP Modules	No DSP	640 DSP48 slices (550 MHz)
Design Environment	Quartus II	ISE + System Generator

TABLE I. Performance comparison between the old Altera board and the new Xilinx FPGA.

The new board is provided with a high flexible development environment that integrates with Matlab's Simulink. This allows the designers to implement block diagrams from library modules (e.g. logical bit operators, lookup tables) in a more friendly way than direct VHDL code.

The current system implementation achieves temperature conversion and image processing in only 190 ns for 76800 pixels. Interpretation of detected hot spots (1-bit 2D matrices) based on CPU requires 15 ms. Com-

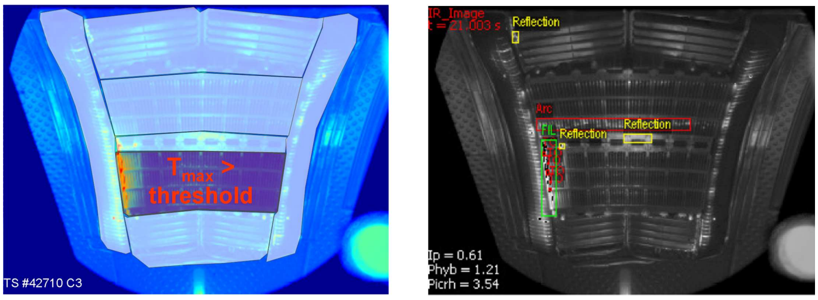

FIG. 1. (color online) Comparison between previous (left) and proposed system (right).

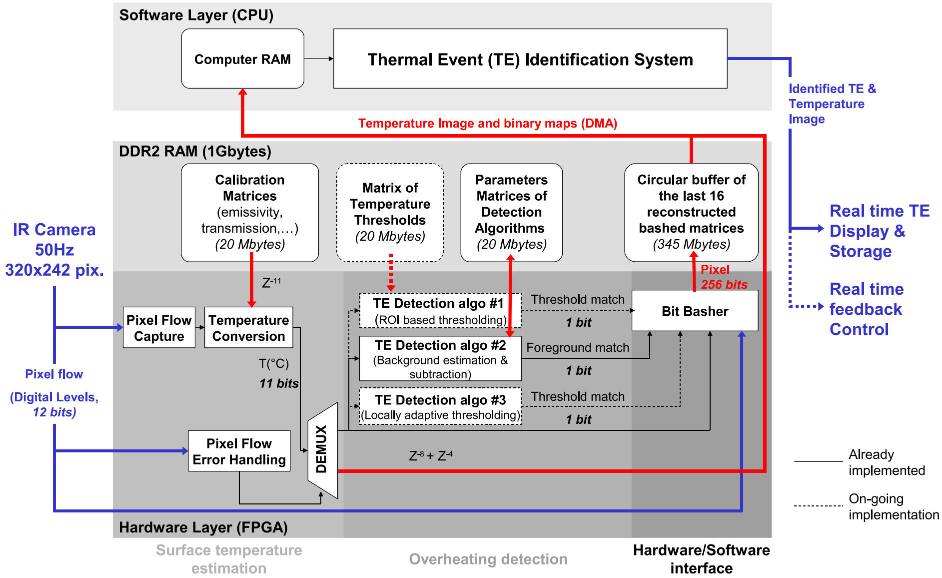

FIG. 2. (color online) System architecture diagram

pared to a ROI-based image analysis system, the new system is able to detect and discriminate different TEs as currently electrical arcing (Arc) and Threshold Overrun (TO). New TEs can be easily added thanks to the modular architecture of both FPGA and TE identification system. Work-in-progress addresses the recognition of others crucial TE as impacts of Fast Ion Losses (FIL) or reflections (see figure 1 right).

VI. CONCLUSION AND OUTLOOK

New industrial FPGA are well-adapted to real-time and complex processing for imaging diagnostics. The major advantages are the ability to exploit parallelism and reconfigurability thus leading to adaptive and fast processing of computer vision algorithms. In this application, a new system based on hardware acceleration has been proposed for the real-time monitoring of PFCs. The global processing speed is currently only limited by the IR camera throughput (i.e. 15 ms per frame). This system is going to be integrated into Tore Supra in parallel with the existing PCS. Experience thereby gained will contribute to the definition of the functionalities of the foreseen visible/infrared system from the equatorial port plug 11 of ITER, which will be involved in the crucial PFC protection function.

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